BCA -03

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Unit-01
ELECTRIC CURRENT

Content of the Unit

1.1 OBJECTIVE

In this chapter we will discuss –

- Electricity, electric charge, voltage and amperage.
- Electric current , resistance & Ohm's law
- Resisivity & conductivity .
- Electromotive force
- Combiniations of resistances in a circuit.
- Power consumption in the electrical circuits.

1.2 INTRODUCTION

What is Electricity?

Electricity is a naturally occurring force that exists all around us. Humans have been aware of this force for many centuries.Greek philosophers noticed that when a piece of amber was rubbed with cloth, it would attract pieces of straw. They recorded the first references to electrical effects, such as static electricity and lightning, over 2,500 years ago.Electricity and magnetism are natural forces that are very closely related to one another.

Electricity has no clear definition since it is so often misused to describe a variety of phenomenon. People commonly use the term electricity to describe **electric charge**, **electric current**, and **electrical energy** . Different definitions of electricity can be found in different places, underscoring our incomplete picture of the complexity of this natural phenomenon. **Electric charge** is a fundamental property of some subatomic particles. Electrons have a electric charge of –1 and a proton has the charge of +1, as do other subatomic particles and ions. **Electric current** describes a flow of electric charge. Electric current is either Direct Current (DC) a single-direction flow, or Alternating Current (AC) which describes a current that repeatedly changes direction. **Electrical energy** is a form of energy present in an electric field or magnetic field, electrical energy is measured in joules. **Electric power** is the name given to electrical energy production and

distribution.

1.2.1 Electric Charge

Electrons:– Electrons are the smallest and lightest of the particles in an atom. Electrons are in constant motion as they circle around the nucleus of that atom. Electrons are said to have a negative charge, which means that they seem to be surrounded by a kind of invisible force field. This is called an **electrostatic field.**

Protons:– Protons are much larger and heavier than electrons. Protons have a positive electrical charge. This positively charged electrostatic field is exactly the same strength as the electrostatic field in an electron, but it is opposite in polarity.In other words, the proton is exactly as positive as the electron is negative.

Like charges repel, unlike charges attract:– Two electrons will tend to repel each other because both have a negative electrical charge. Two protons will also tend to repel each other because they both have a positive charge. On the other hand, electrons and protons will be attracted to each other because of their unlike charges.

Since the electron is much smaller and lighter than a proton, when they are attracted to each other due to their unlike charges, the electron usually does most of the moving. This is because the protons have more mass and are harder to get moving. Although electrons are very small, their negative electrical charges are still quite strong. Remember, the negative charge of an electron is the same as the positive electrical charge of the much larger in size proton. This way the atom stays electrically balanced.

Another important fact about the electrical charges of protons and electrons is that the farther away they are from each other, the less force their electric fields have on each other. Similarly, the closer they are to each other, the more force they will experience from each other due to this invisible force field called an electric field.

The unit of electric charge is the Coulomb (abbreviated C). Ordinary matter is made up of atoms which have positively charged nuclei and negatively charged electrons surrounding them. Charge is quantized as a multiple of the electron or photon charge:

⊕ Proton charge $e = 1.602 \times 10^{-19}$ coulombs

⊖ Electron charge $-e = -1.602 \times 10^{-19}$ coulombs

The influence of charges is characterized in terms of the forces between them (Coulomb's law) and the electric field and voltage produced by them.

1.2.2 Amperage

It is very important to have a way to measure and quantify the flow of electrical current. When current flow is controlled it can be used to do useful work.

The flow of electrons is measured in units called **amperes**. The term **amps** is often used for short. An amp is the amount of electrical current that exists when a number of electrons, having one coulomb (ku'-lum) of charge, move past a given point in one second. A **coulomb** is the charge carried by 6.25×10^{18} electrons. 6.25×10^{18} is scientific notation for 6,250,000,000,000,000,000.An **ammeter** is this instrument and it is used to indicate how many amps of current are flowing in an electrical circuit.

1.2.3 Voltage

We also need to know something about the force that causes the electrons to move in an electrical circuit. This force is called **electromotive force**, or **EMF**. Sometimes it is convenient to think of EMF as electrical pressure. In other words, it is the force that makes electrons move in a certain direction within a conductor.

The rate of flow of electric charge is called electric current and is measured in Amperes.

1.3 ELECTRIC CURRENT

Electricity is a term used to describe the energy produced (usually to perform work) when electrons are caused to directional (not randomly) flow from atom to atom. In fact, the day-to-day products that we all benefit from, rely on the movement of electrons. This movement of electrons between atoms is called **electrical current**.

When a cireuit is connected to a source to EMF (electromotive force), the free electrons in the con-

ductor starts to move in a definite directions along with their random motion. In this way charge flows in the circuit as long as the source of emf is connected to the circuit. Therefore, rate flow of charge (electric) through any section of a wire is defined as "electric current" (I). Thus,

$$I = \frac{\text{Total charge flowing}}{\text{Time taken}} = \frac{q}{t} \qquad \text{.....(1)}$$

where total charge q = no. of carriers × charge = ne

$$\therefore \qquad I = \frac{ne}{t} \qquad \text{.....(2)}$$

If δQ amount of charge flows is the cirecuit in a small time intonal δt then the current

$$I = \lim_{\delta t \to 0}\left(\frac{\delta Q}{\delta t}\right) = \frac{dQ}{dt} \qquad \text{.....(3)}$$

The direction is which the positive charge will flow gives the direction of conventional current, which is opposite to the electronic current due to the flow of electrons. The current is a scalar quantity even the direction is associated with it because the laws of ordinary algebra is used to add electric current. Practical unit of current is amper (A) and is equal to coulomb per second. When one coulomb charge flows is one second the current is called one ampere, i.e.,

$$1 \text{ Ampere} = \frac{1 \text{ Coulomb}}{1 \text{ Sec.}} = 1 CS^{-1}$$

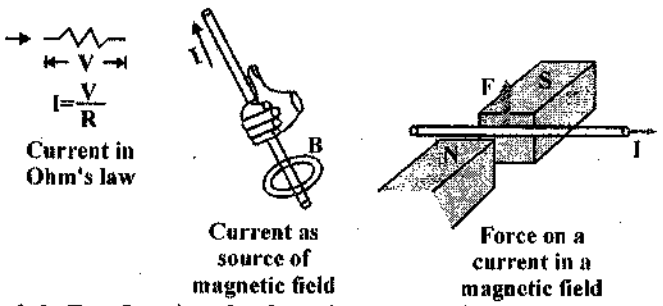


Figure1.1: Production fo electric current in different ways.

SI unit of current is defined from the magnetic effect of current. According to this definition- One ampere is that current which when flows two infinitely long thin conductors parallel to each other and 1 m apart, produces a force of 2×10^{-7} N/m between there.

In a metallic conductor, free electrons are carriers of electricity and hence electrons constitute the electric current. 6.25×10^{18} electrons crossing per second through any section of a conductor given rise to a current of 1A.

Proof:

$$\because \; I = \frac{ne}{t} \qquad \Rightarrow \qquad n = \frac{It}{e}$$

Setting I = 1Amp.; t = 1 Sec, and $e = 1.6\times10^{-19}$ $\Rightarrow$ $n = 6.25\times10^{18}$

Ex.01 A charge of 90 columb is flowing through a silver wire for 0.5 minute. Calculate the current in wire.

Solution: Given data $q = 90$ columb, $t = 0.5$ minute $= 0.5\times 60 = 30$ sec.

we know that $q = i\times t$

$$\therefore \qquad 90 = i\times 30$$

$$i = \frac{90}{3} = 3 \text{ Amp.}$$

Ex.02 A current of 40 miliampere is flowing through a copper wire. Calculate the total charge that passes through in 2 sec. Also find the number of electrons that pass through in same time.

Solution: Given data $i = 40$ miliampere $= 40\times10^{-3}$ Amp.; $t = 2$ sec.

We know that $q = i\times t$

$$q = (40\times10^{-3})\times2$$

$$q = 80\times10^{-3}$$

$$q = 80 \text{ mili columb.}$$

The number of electron $q = n\times e$

$$80\times10^{-3} = n\times(1.6\times10^{-19})$$

$$n = \frac{80\times10^{-3}}{1.6\times10^{-19}}$$

$$n = 5\times10^{17} \text{ electrons}$$

Ex.03 How long does it take 50μC of charge to pass a point in circuit if the current is 15 mA.?

Solution: Given data $q = 50 = 50\times10^{-6}$; $i = 15\,\text{mA} = 15\times10^{-3}$ Amp.

We know that $q = i\times t$

$$50\times10^{-6} = 15\times10^{-3}\times t$$

$$t = \frac{50\times10^{-6}}{15\times10^{-3}} = 3.33\times10^{-3}$$

$$t = 3.33 \text{ sec.}$$

Ex.04. The current in an electron beam of a CRO is 200μA. How many electrons strike the screen per second?

Solution: If the number of electrons passing across any cross section of the beam per second is n, then charge flowing per second is $n\times e$.

So current $I = n\times e$

or $$n = \frac{I}{e}$$

$\therefore$ $$n = \frac{200\times10^{-6}}{1.6\times10^{-19}} = 1.25\times10^{15} \text{ per second.}$$

1.4 MEAN FREE PATH, RELAXATION TIME AND DRIFTVELOCITY

Every metal has a large number of free electrons and these free electrons behave like the molecules of a gas filled in a closed chamber. The total number of free electrons per cubic volume of a conductor is around 10^{29}. These free electrons move randomly with a very high velocity (~10^5 m/s), but the directions of their motions are zig-zag, i.e., randomly distributed. During the motion, the free elctrons collide with the material ions continuously which cauuses the change their direction of motion.

Thus the average distance covered by free elecrons between two successive collisions is called "mean free path" of electron. The time interval taken by the electron in two successive collision is called "relaxation time".

In the presence of external electric field, free electrons experience an additional electric field inside the

conductor, which further accelerates the motion of electrons. During the motion, free electrons collide again and again and thus extra velocity so gained is destroyed between these collisions. But free electrons in order to their random motion gain a small velocity towards the positive end of conductor. Therefore, the drift velocity is an average velocity (~10^{-4} m/s) with which free electrons get drifted towards the positive end of conductor under the influence of an external electric filed.

1.5 RELATION BETWEEN DRIFT VELOCITY AND CURRENT OF FREE ELECTRONS

Suppose a conductor of length 'l' and of uniform area of cross section A is connected to a battery such that an external electric filed is applied is setup within the conductor. With this, free electrons starts to move with drift velocity as shown in Figure (1.2).

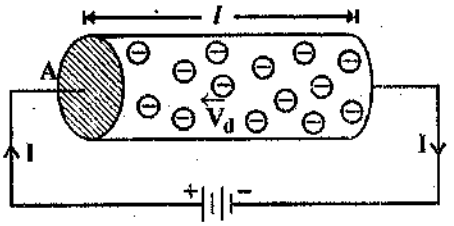


Figure:1.2

If the number of free electrons per unit volume of conductor wire is n, then the total number of free electrons in the conductor will be $(A.l.n)$. Therefore, the total charge in the conductor will be

$$q = (A.l.n).e$$

Time taken by the free electrons to cross the conductor is

$$t = \frac{l}{v_d}$$

Hence the current

$$I = \frac{q}{t},$$

$$I = \frac{(A.l.n).e}{l/v_d},$$

$$I = Anev_d.$$

This is the relation between drift velocity and electric current. Since A, n and e are constants, thus current flowing in conductor is directly proportional to drift velocity, i.e.,

$$I \propto v_d$$

Ex.05 The number density of conduction electron in a copper conductor is $8.5\times10^{23}\,m^{-3}$. How long does an electron take to drift from one end to wire 3 meter long to its other end? The area of cross-section of wire is $2\times10^{-6}\,m^2$ and carrying a current of 3.0 Amp.

Solution: Given data $n=8.5\times10^{28}$, $l=3$ meter, $A=2\times10^{-6}\,m^2$, $i=3$ Amp.

We know that $i = A\times n\times e\times v_d$

$$v_d = \frac{i}{A\times n\times e}$$

$$v_d = \frac{3}{2\times10^{-6}\times8.5\times10^{28}\times1.6\times10^{-19}}$$

$$v_d = 1.1\times10^{-4}$$

Time taken by electron

$$t = \frac{1}{v_d}$$

$$t = \frac{1}{1.1\times10^{-4}} = 2.72\times10^{4} \text{ sec.}$$

1.6 RESISTANCE

There is another important property that can be measured in electrical systems. This is **resistance**, which is measured in units called **ohms**. Resistance is a term that describes the forces that oppose the flow of electron current in a conductor. All materials naturally contain some resistance to the flow of electron current. We have not found a way to make conductors that do not have some resistance. The resistance of a conductor implies the "opposition to the free electrons drift from one end to another end of the conductor along with the random motion" when a potential difference is applied across the conductor, an electric field is set up across its two ends. Due to this, these free electrons collide with the ions/atoms during their motion and thus motion is opposed. The opposition offered by the atoms as a result of which the electrons are slowed down is termed as resistance of the conductor.

1.7 OHM'S LAW

It is most fundamental law of electricity and was given by George simon ohm is 1828. Ohm applied different potential difference across a conducting wire and determined the amount of current flowing through it. He gave a relation between potential difference accross the conductor and amount of current flowing through it. It states that "the physical condition remains unchanged, the current flowing through a conductor is always directly proportional to the potential difference across its two ends. Thus -

$$V \propto I$$

$$V = RI \qquad \text{.....(5)}$$

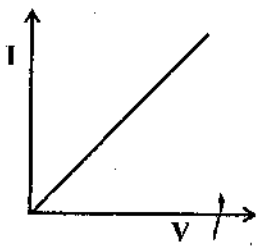


Figure: 1.3

where R is proportionality constant and known as Resistance. Its value depends upon the nature of conductor, its dimensions and the physical conditions. It is in dependent of the values of I & V. If a graph between the applied polential difference V and current I is plotted, a straight line is obtained passes through the origin.

Ohm's law is valid only for metallic conductors, in which there are free electons.

Ex.06 A potential difference of 200V is applied across the ends of conductor of resistance 50Ω. Calculate the number of electrons flowing through it in 1 second.

Solution: Given data $V = 200$ Volt., $R = 50\Omega$, $t = 1$

We know that $V = i \times R$

$$200 = i \times 50$$

$$i = \frac{200}{50} = 4 \text{ Amp.}$$

Number of electron

Q $q = i \times t = n \times e$

$$\therefore \quad n = \frac{i \times t}{e}$$

$$n = \frac{4 \times 1}{1.6 \times 10^{-19}} = 2.5 \times 10^{19}$$

Ex.7 When a potential difference of 2.0 Volt is applied across a resistance wire it produces 0.5 Amp. current. Calculate its resistance.

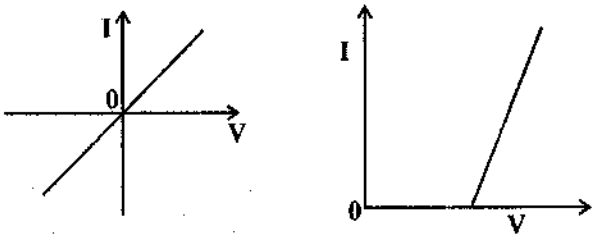
Solution: Given data $V = 2$ Volt.; $i = 0.5$ Amp.

We know that $V = i \times R$

$$R = \frac{V}{i} \qquad \therefore \quad R = \frac{2}{0.5} = 4\Omega$$

Relationship between I and V for various devices are shown in following graphs for illustration.

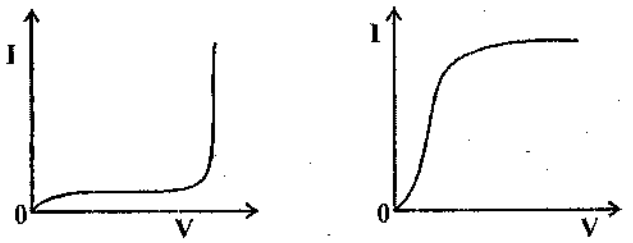
(i) Current–Voltage relationship for Ohmic conductor and water voltameter.



(a) Ohmic conductor **(b) Water voltameter**

Figure: 1.4

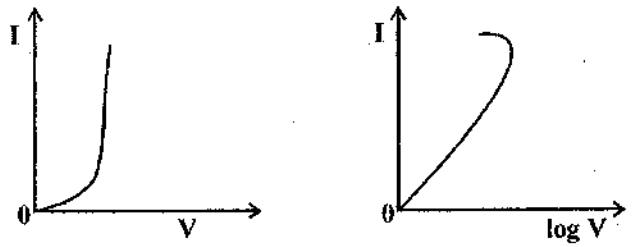
(ii) Current–Voltage relationship for Gas discharge tube and Thermionic diode



(a) Gas discharge tube **(b) Thermionic diode**

Figure: 1.5

(iii) Current-Voltage relationship for Junction diode and Thermistor.



(a) Junction diode **(b) Thermistor**

Figure: 1.6

1.8 RESISTIVITY AND CONDUCTIVITY

With the knowledge of Ohm's law, given by equation (5), the resistance of a conductor is defined as the ratio of the potential difference to the current flowing through it.

$$R = \frac{V}{I} \qquad \text{.....(6)}$$

SI unit of resistance is ohm. It is denoted by Ω. The resistance of a conductor is said to be one ohm, if one ampere of current flows through it, when a potential difference of one volt is applied across it.

1.8.1 Resistivity

The resistance of a conductor depends upon the following factors:

(i) Length of Conductor: It is directly proportional to length of the conductor; *i.e.* more is the length of wire, more will be its resistance.

$$R \propto l \qquad \text{.....(7)}$$

(ii) Cross-sectional area or thickness of the conductor: It is inversely proportion to the area of cross-sections of the conductor. More is the thickness of wire, more is its area of cross-section and less is its resistance thus

$$R \propto \frac{1}{A} \qquad \text{.....(8)}$$

(iii) Material of a conductor: It the conductor/wire of same length, and same thickness are made from different materials then their resistance will be different. Thus the resistance of a wire also depends on the nature of its material. For example the resistance of silver, copper wire is very small but for iron, nickle, nichrome, constantan and manganin wire, it is very large.

Combining (7) and (8) we get

$$R \propto \frac{l}{A}$$

$$R = \rho \frac{l}{A} \qquad \text{.....(9)}$$

where ρ is proportionality constant and called as electrical Resistivity or Specific Resistance of the conductor.

If $l = 1$, $A = 1$ then $\rho = R$

Hence, the resistivity or specific resistance of the material of a conductor is the resistance offered by a wire of unit length and unit cross-section area.

It S.I., the unit of resistivity is ohm. meter. The electrical resistivity of substances varies over a wide range.

1.8.2 Conductance and Conductivity

Conductance: The reciprocal of a conductor is called its conductance is denoted by G.

$$G = \frac{1}{R} \qquad \text{.....(10)}$$

S.I. unit of conducatance is **Ohm^{-1}**, which is also called **Mho.**

Conductivity: Reciprocal of resistivity is called conductivity. It is denoted by σ

$$\sigma = \frac{1}{\rho} = \frac{1}{RA}$$

S.I. unit of conductivity $\sigma = \frac{1}{\text{ohm meter}} = \text{ohm}^{-1}\,\text{meter}^{-1} = \text{mho meter}^{-1}$

1.8.3 Temperature Dependance Resistivity

The resistance of a conductor depends upon the temperature. As the temperature increase, the random motion of free-electron also increases. If the number density of charge carriers, remains constant, then the increase of random motion increases the resistivity and so the resistance. The variation of resistance with temperature is given by following relation:

$$R_t = R_0(1 + \alpha t + \beta t^2)$$

where R_t and R_0 are the resistance at t°C and 0°C respectively. α, β are constant. The constant β is very small in comparison to the α for a small variation of temperature.

$$R_t \approx R_0(1+\alpha t)$$

$$\alpha = \frac{R_t - R_0}{R_0 t} \qquad \text{.....(11)}$$

This constant α is called temperature coefficient of resistance of the material.

If $R_0 = 1\Omega$; $t = 1°C$ then $\alpha = (R_t - R_0)$

Thus the temperature coefficient of a resistance is defined as the increase in resistance of a conductor of resistance 1Ω on raising its temperature by 1°C.

For most of the metals, the value of α is nearly $\frac{1}{273}$ per °C. Hence

$$R_t = R_0\left(1+\frac{1}{273}t\right) = R_0\left(\frac{273+t}{273}\right) = R_o\frac{T}{273} \qquad \text{.....(12)}$$

where T is the absolute temperature of the conductor

$\therefore \quad R_t \propto T$

Thus the resistance of a pure metal wire is directly proportional to its absolute temperature.

Ex.08 Calculate the electrical conductivity of the material of a conductor of length 3 meter, area of cross-section 0.02 mm2 having a resistance of 2 ohm.

Solution: Given data $l = 3$ meter ; $A = 0.02 = 0.02\times10^{-6}$ meter; $R = 2\Omega$

Since, conductivity, $\sigma = \frac{1}{\rho}$,

we have $\sigma = \frac{1}{RA} = \frac{3}{2\times0.02\times10^{-6}} = 7.5\times10^{7}\ sm^{-1}$

Ex.09 A current of 0.2 Amp. is passed through a coil of iron wire which has a cross-sectional area of 0.01 cm2. If the resistivity of iron is $14\times10^{-8}\ \Omega - m$ and the potential difference across the ends of coil is 21 volts, what is length of the wire? Calculate conducitivity of the wire.

Soluiton: Given data $i = 0.2$ Amp. $V = 21$ Volt., $\rho = 14\times10^{-8}\ \Omega - m$;

$$A = 0.01\text{cm}^2 = 0.01\times10^{-4}\text{m}^2$$

We know that $V = i \times R$

$$R = \frac{V}{i}$$

$$R = \frac{21}{0.2} = 105\Omega$$

Q $$R = \rho.\frac{l}{A}$$

$$105 = \frac{14\times10^{-8}\times1}{0.01\times10^{-4}}$$

$$l = \frac{105\times0.01\times10^{-4}}{14\times10^{-8}} = 750\text{ meter}$$

The conductivity is reciprocal of resistivity

$$\therefore \quad \sigma = \frac{1}{\rho} \qquad \sigma = \frac{1}{14\times10^{-8}} = 7.14\times10^{6}$$

Ex.10 The resistance of a tungsten filament at 150°C is 133 Ohm. What will be its resistance at 500°C.? The temperature coefficient of resistance of tungsten is 0.0045 per °C.

Solution: If the resistance of wire at 0°C be R_0 and at t°C be R_t, then

$$R_t = R_0(1+\alpha t)$$

$$R_0 = \frac{R_t}{1+\alpha t}$$

Hence the resistance of filament at 150°C is 133 Ω thus resistance at 0°C is

$$R_0 = \frac{133}{1+0.0045\times150}$$

$$R_0 = 79.0\,\Omega$$

Resistance of filament at 500°C will be

$$R_{500} = \frac{R_0}{1+\alpha.t}$$

$$R_{500} = \frac{79}{1+0.0045\times500}$$

$$R_{500} = 275\,\Omega$$

Ex.11 A conducting wire has a radius of 0.5 mm and length 2.0 meter. If its resistance is 0.05 Ohm, determine its resistivity.

Solution: Given data $R = 0.05$ Ohm, $A = \pi r^2 = \pi(0.5\times10^{-3})^2$; $l = 2.0$ meter

Resistivity $\rho = \frac{RA}{l}$

$$\therefore \quad \rho = \frac{0.05\times\pi\times(0.5\times10^{-3})^2}{2.0}$$

$$\rho = 196.25\times10^{-10}$$

$$\rho = 1.96\times10^{-8} \text{ Ohm-meter}$$

x.12 Two conductors of the same material have the same length. One conductor is a solid wire of neter 1.0 mm while the other is a hollow tube havign external and internal diameters as 2.0 mm and nm respectively. Determine the ratio of their resistances.

ı: Resistance $R = \rho\frac{l}{A}$

luctor $r = \frac{1.0}{2} = 0.5$ mm

$$R_1 = \rho\frac{l}{\pi(0.5\times10^{-3})^2}$$

For hollow conductor $r_1 = \frac{2.0}{2} = 1.0$ mm, $r_2 = \frac{1.0}{2} = 0.5$ mm.

$$R_2 = \rho \frac{l}{\pi(r_1^2 - r_2^2)}$$

$$R_2 = \rho \frac{l}{\pi[(1.0)^2 - (0.5)^2] \times 10^{-6}}$$

$$\therefore \quad \frac{R_1}{R_2} = \frac{(1.0 - 0.25) \times 10^{-6}}{0.25 \times 10^{-6}} = \frac{0.75}{0.25} = \frac{3}{1}$$

Ex.13 Calculate the electrical conductivity of the material of a conductor of length 3 meter, area of cross-section 0.02 mm2 having a resistance of 2 Ohm.

Solution: Given data $l = 3$; $A = 0.02\, mm^2 = 0.02 \times 10^{-6} m^2$; $R = 2\Omega$

Since, conductivity, $\sigma = \frac{1}{\rho}$, we have

$$\sigma = \frac{l}{RA} = \frac{3}{2 \times 0.02 \times 10^{-6}} = 7.5 \times 10^7 Sm^{-1}$$

Ex.14 A wire has resistance of 32Ω. It is melted and drawn into a wire of half of its original length. Calculate the resistance of the new wire. What is percentage change in resistance?

Solution: Let l and r be length and radius of the wire respectively. If ρ is resistivity of the material of the wire, then.

$$R = \rho \frac{l}{A} = \rho \frac{l}{\pi r^2}$$

Suppose that the radius of wire becomes l', when wire is drawn into a wire of length $l' = l/2$ by melting it. Since the volume of the wire must remain unchaged, we have.

$$\pi r'^2 l' = \pi r^2 l$$

or $\quad \pi r'^2 (l/2) = \pi r^2 l$

or $\quad r'^2 = 2r^2$

If R' is new value of the resistance of the wire, then

$$R' = \rho \frac{l'}{A'} = \rho \frac{l'}{\pi r'^2} = \rho \frac{l/2}{\pi(2r^2)} = \frac{1}{4}\left(\rho \frac{1}{\pi r^2}\right)$$

we have

$$R' = \frac{R}{4} = \frac{32}{4} = 8\Omega \qquad (\text{Q } R = 32\Omega)$$

Therefore, percentage change in resistance

$$= \frac{32 - 8}{32} \times 100 = 75\% \text{ (decrease)}$$

Ex.15 The resistance of a conductor is 6Ω at 50°C and 7Ω at 100°C. Calculate ture coefficient of resistance of the material. Find the resistance of the conductor a

Solution: Given data $\theta_1 = 50°C$; $R_1 = 6\Omega$; $\theta_2 = 100°C$; $R_2 = 7\Omega$

Mean temperature coefficient of resistance of the material,

$$\alpha = \frac{R_2 - R_1}{R_1 \times (\theta_2 - \theta_1)};$$

$$\alpha = \frac{7-6}{6\times(100-50)};$$

$$\alpha = \frac{1}{6\times 50} = \frac{1}{300}\ {}^{o}C^{-1}$$

If R_0 is resistance of the conductor at 0°C, then

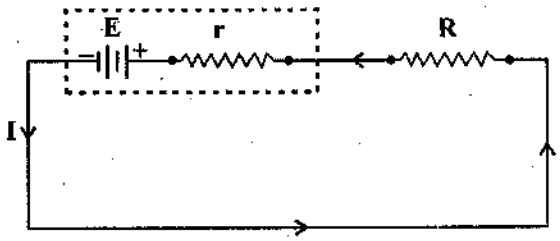
$$R_1 = R_0(1+\alpha\theta)$$

or $$R_0 = \frac{R_1}{1+\alpha\theta} = \frac{6}{1+\frac{1}{300}\times 50} = \frac{36}{7} 5.143\Omega$$

1.9 ELECTRO MOTIVE FORCE (EMF)

A constant current can be maintained in a closed circuit through the use of a source of energy, called an electromotive force. A source of e.m.f. is any device (such as battery or generator) that will increase the potential energy of charges circulating in a circuit. Actually e.m.f. is not a force but energy or work done per unit charge like potential. SI unit of e.m.f. is the volt.

When current is drawn from a cell by connecting it to an external circuit, the cell is said to be in closed circuit. If current is not drawn, then the cell is said to be in open circuit. When current is not drawn from the cell i.e., cell is in open circuit, the potential difference E between the terminals of the cell is called electromotive force (e.m.f.). When current is drawn form the cell in the external circuit. i.e., external circuit is closed, the potential difference between the terminals of the cell at that time is called terminal voltage. It is also equal to the potential difference across the external resistance. It is generally represented by V. The e.m.f. E of a cell in a closed circuit is equivalent to the work done for the flow of unit positive charge through the external and internal resistance whereas potential difference or terminal voltage is equivalent to the work done for the flow of unit positive charge through the external resistance only. Thus E is always greater than V and their difference (E–V) is equal to the potential drop across the internal resistance of the cell.



Figrue:1.7

ɔr a generator can be represented by a source of e.m.f. 'E' with an internal resistance 'r' ɔd in series. When no current is drawn the internal resistance is ineffective and the potential between the electrodes is equal to the e.m.f. When the external circuit draws a current I, ɔential drop (Ir) on the internal resistance so that the potential difference between its ɔes (E–Ir) = V. The emf (E) is the amount of work done in driving a unit positive charge ɔ circuit (external and internal) while the potential difference V in the closed circuit is ɔ done in driving a unit positive charge through the external resistance only. If an ɔ is connected to the cell or generator and a current I flows through it, then

$$E = IR + Ir \qquad \text{.....(13)}$$

while $V = IR$ or $I = \frac{V}{R}$

$\therefore \quad E = V + Ir$

or $$r = \frac{(E - V)}{I} \qquad \text{.....(14)}$$

Substituting the value of I

$$r = \frac{(E - V)}{V/R} = \left(\frac{E - V}{V}\right) R \qquad \text{.....(15)}$$

1.10 COMBINATION OF RESISTANCE

Resistance can be combined in the following two ways in a circuit:

(a) In series and

(b) In parallel.

1.10.1 Resistance in Series

Two or more resistance are said to be connected in series, if same current passes through each resistance, when some potential difference is applied across the combination.

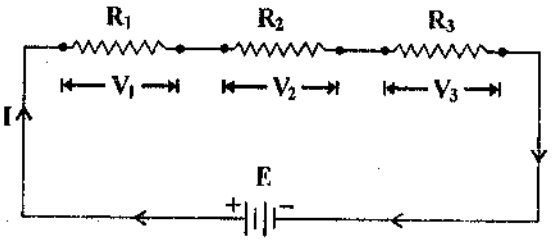


Figure: 1.8

Above Figure (1.8) shows the combination of three resistance R_1, R_2 & R_3 and their equivalent resistance is R_s. Equivalent resistance is that resistance which when connected in place of the combination of resistances, no changes of current takes place in the circuit. If a battery of e.m.f. "E" is connected across the series combination, the same current I will pass through each of them. If V_1, V_2 & V_3 are the values of potential difference across R_1, R_2, R_3 then according to Ohm's law.

$$V_1 = IR_1; \quad V_2 = IR_2; \quad V_3 = IR_3$$

and if total e.m.f. of circuit is equal to the total potential difference.

$$E = V_1 + V_2 + V_3 \qquad \text{.....(16)}$$

$$E = IR_1 + IR_2 + IR_3$$

$$E = I(R_1 + R_2 + R_3)$$

$$E = IR_S$$

where $R_S = R_1 + R_2 + R_3$ equivalent resistance.

Thus, the equivalent resistance of the series combination is equal to the sum of individual resistances.

1.10.2 Resistance in Parallel

Two or more resistance are said to connect in parallel. If potential difference across each of them is equivalent to the applied potential difference.

Figure (1.9) shows the combination of three resistance R_1, R_2 & R_3 in parallel. If a battery of e.m.f.

"E" is connected across theparallel combination in the potential difference across each resistance will be equal to E, the e.m.f. of the battery. If I_1, I_2 & I_3 are the values of current through the resistance R_1, R_2 & R_3 respectively, then the current is main circuit.

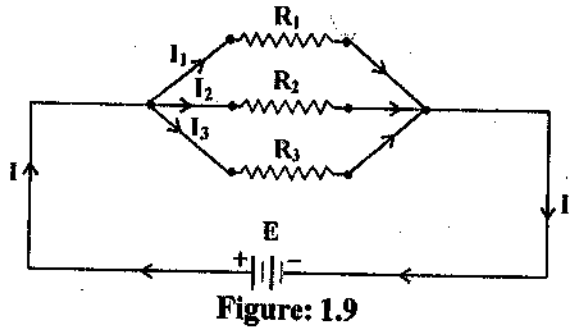


Figure: 1.9

$$I = I_1 + I_2 + I_3 \qquad \text{.....(17)}$$

Q The potential difference across each resistance is E, therefore applying Ohm's law

$$E = I_1 R_1 = I_2 R_2 = I_3 R_3$$

$$I_1 = \frac{E}{R_1}, \quad I_2 = \frac{E}{R_2}; \quad I_3 = \frac{E}{R_3}$$

Therefore equation (17) becomes.

$$I = E\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) \qquad \text{.....(18)}$$

If R_P is the equivalent resistance to parallel combination of R_1, R_2 *and* R_3, i.e. R_P allows the same current I to flow through it, when the battery of e.m.f. E is connected.

$$E = IR_P \qquad I = \frac{E}{R_P}$$

$\therefore$ with equation (17) and (18)

$$\frac{1}{R_P} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \qquad \text{.....(19)}$$

Thus, when the resistance are connected in parallel, the reciprocal of the equivalent resistance of the parallel combination is equal to the sum of the reciprocal of individual resistance. It is also noted that the value of equivalent resistance is always less than the value of smallest individual resistance and therefore resistance are connected in parallel if the resistance in the circuit is to be reduced.

Ex.16 Three resistances 2Ω, 4Ω and 5Ω are connected in parallel. What is the total resistance of combination if the combination is connected to a battery of e.m.f. 20V. Calculate the current through each resistor.

Solution: Given data $R_1 = 2\Omega$, $R_2 = 4\Omega$, $R_3 = 5\Omega$, $V = 20$ volt.

Since resistances are connected in parallel hence equivalent resistance

$$\frac{1}{R} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}$$

$$\frac{1}{R} = \frac{1}{2} + \frac{1}{4} + \frac{1}{5} = \frac{19}{20}$$

$$R = \frac{20}{19}\Omega$$

Now current through resistance R_1

$$i_1 = \frac{V}{R_1} = \frac{20}{2} = 10 \text{ Amp.}$$

Current through resistance R_2

$$i_2 = \frac{V}{R_2} = \frac{20}{4} = 5 \text{ Amp.}$$

Current through resistance R_3

$$i_3 = \frac{V}{R_3} = \frac{20}{5} = 4 \text{ Amp.}$$

Ex.17 Calculate the equivalent resistance and total current for following circuit.

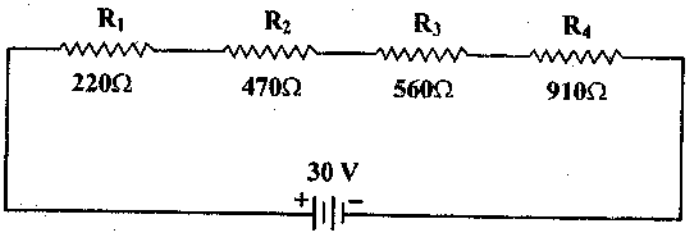


Figure: 1.10

Solution: Given data $R_1 = 220\Omega$; $R_2 = 470\Omega$; $R_3 = 560\Omega$; $R_4 = 910\Omega$

Since ressitances are joined in series

$$R = R_1 + R_2 + R_3 + R_4$$

$$R = 220 + 470 + 560 + 910 = 2160\Omega$$

$$\text{Total current in circuit} = \frac{\text{Potential Difference}}{\text{Total Resistance}} = \frac{30}{2160} = 0.013 \text{ Amp.}$$

Ex.18 Determine the following in the given circuit. (i) Total resistance of the circuit and (ii) Current flowing through the resistor of 10 Ohm.

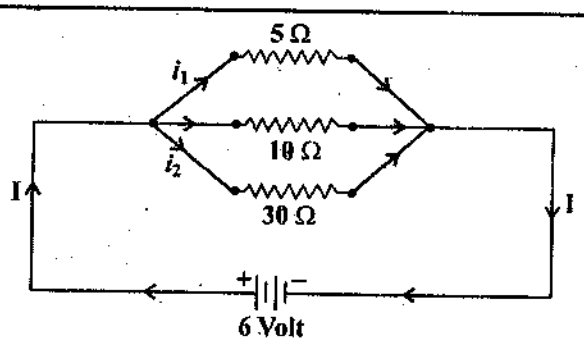


Figure: 1.11

Solution: The three resistors are connected in parallel. If R is the their equivalent resistance, then

$$\frac{1}{R} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}$$

$$\frac{1}{R} = \frac{1}{5} + \frac{1}{10} + \frac{1}{30}$$

$$\frac{1}{R}=\frac{6+3+1}{30}=\frac{10}{30}$$

$$R=\frac{30}{10}=3\Omega$$

Current following through the resistance of 10 Ohm will be

$$I_2=\frac{V}{R_2}=\frac{6}{10}=0.6 \text{ Amp.}$$

1.11 CURRENT IN SINGLE LOOP

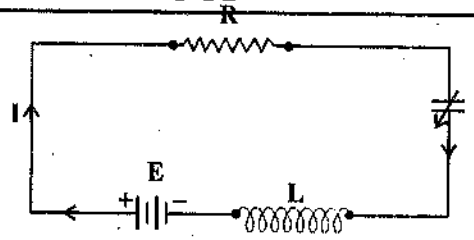


Figure: 1.12

The closed path of the current in a circuit having component like resistance, inductance, capacitance etc. is called loop. In a single loop the current is same at every point, because of consummation of charges (neither the charges can be destroyed or created). There fore for a particular time duration, the amount of charges enters the component of the circuit is the same amount of changes leave it. Current starts from the the terminal is not used up unless it does not reach to the –ve terminal.

1.12 ELECTRICAL POWER CONSUMPTION

Electric current is produced by the flow of free electrons in conductors, for which a source of e.m.f. is used to flow the electrons. During their motion these free electrons starts collide with the atoms of conductors and thus produces obstacles in their flow is called resistance. Due to the Collisions, some of the energy is lost which increases the kinetic energy of electrons and appears in the form of heat. For example, in daily life like heater, electric iron, electric kettle, electric oven etc. consumes electrical energy.

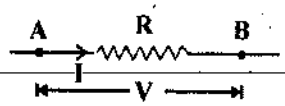


Figure: 1.13

Consider a resistance R, across which the potential difference V is applied. According to ohm's law, current I flowing thought the resistor is given by

$$V=RI \qquad \text{.....(20)}$$

Suppose the steady current I flows through the resistor for a time t, the amount of total charges flows through it in t time is given by

$$q=It \qquad \text{..... (21)}$$

If current is flowing from end A to B, then potential V at end A is higher than that of end B. From the definition of potential difference, "if one joule work is done is carrying a charge of one coulomb through the conductor, then the potential difference across the conductor will be one volt", i.e., if a unit charge is made across the resistor from the end B to A (lower and potential to higher end potential), work done is equal to V.

Therefore, if current I flows for time t, i.e., total charges. It crosses the resistor from end A to B then electical energy consumed is given by–

$$W=V(It)=VIt \qquad \text{.....(22)}$$

Q $V = IR$

$\therefore \quad W = I^2 Rt$ .....(23)

The rate at which the work is done in maintaining the electic current in a circuit is called electrical power of circuit.

If P is electric power of the circuit, then

$$P = \frac{W}{t} \quad .....(24)$$

Using equation (24),

$$P = VI \quad .....(25)$$

and also from eq. (25), we have

$$P = I^2 R \quad .....(26)$$

S.I. unit of electric power is **Watt.**

1 Watt = 1 volt × 1 ampere

The electrical power of a circuit or a device is said to be one watt, if one ampere of current flows through it, when a constant potential difference of 1 volt is applied.

Equation (26) can be written as $W = Pt$

S.I. Unit of work in electrical circuit is joule but another unit called watt-hour.

1 watt-hour = 1 watt × 1 hour.

The bigger unit of electrical energy is kilowatt-hour. It is also known as Board of Trade Unit.

1 Kilowatt hour = 10^3 watt hour

$$1\text{KWH} = 10^3 (\text{JS}^{-1}) \times (60 \times 60^3)$$

$$= 3.6 \times 10^6 \text{ J}$$

The electrical energy consumed in KWH is given by

$$\text{W(in KHH)} = \frac{\text{V (Volt)} \times \text{I (Ampere)} \times t \text{ (Hours)}}{1000}$$

Net power is series $\frac{1}{P} = \frac{1}{P_1} + \frac{1}{P_2} + \frac{1}{P_3} + ...$

Net power in parallel $P = P_1 + P_2 + P_3 + ...$

Chart for SI multiples for watt (W).

Ex.19 A single-loop circuit contains two external resistors and two seats of e.m.f. as shown in Figrue (1.14). The internal resistances of the batteries have been neglected (a) Calculate the current in the circuit. (b) What is the power lost in each resistor?

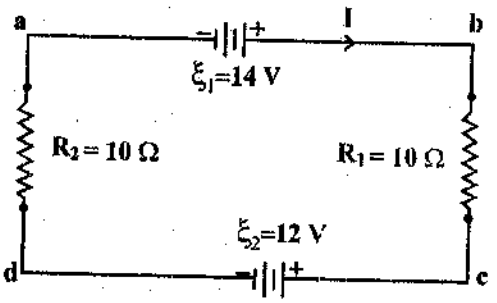


Figure:1.14

Solution: (a) There are no junctions in this single-loop circuit, and so the current is the same in all

elements.

Let us assume that the current is in the clockwise direction as shown in Figure (1.14) Traversing the circuit in the clockwise direction, starting at point a, we see that $a \to b$ represents a potential increase of $+\xi_1$, $b \to c$ represents a potential decrease of $-IR_1$, $c \to d$ represents a potential decrease of $-\xi_2$ and $d \to a$ represents a potential decrease of $-IR_2$.

Applying Kirchhoff's second rule gives

$$\sum_i V_i = 0$$

$$\xi_1 - IR_1 - \xi_2 - IR_2 = 0$$

Solving for I and using the values given in Figrue, we get

$$I = \frac{\xi_1 - \xi_2}{R_1 + R_2}$$

$$I = \frac{6V - 12V}{8\omega + 10\Omega} = -\frac{1}{3}\text{Amp.}$$

The negative sign for I indicates that the current is opposite the assumed direction, or counterclockwise.

(b) $$P_1 = I^2 R_1 = \left(\frac{1}{3}A\right)^2 (8\Omega) = \frac{8}{9}\text{ W}$$

$$P_2 = I^2 R_2 = \left(\frac{1}{3}A\right)^2 (10\Omega) = \frac{10}{9}\text{ W}$$

Hence, the total power lost is $P_1 + P_2 = 2$ W. The 12 V battery delivers power $I\xi_2 = 4$ W. Half of this power is delivered to the external resistors. The other half is delivered to the 6 V battery, which is being charged by the 12 V battery. If we had included the internal resistances of the batteries, some of the power would be dissipated as heat in the batteries, so that less power would be delivered to the 6 V battery.

Ex.20 There are following load on a circuit through a supply meter:

(i) Six lamps of 40 watts each working for 4 hours per day.

(ii) Two fluorescent tubes 125 watt each working for 2 hour's per day.

(iii) One 1000 watt heater working for 3 hour's per day.

If each unit of energy cost 70 paisa, what will be the electricity bill for month of April.

Solution: Total wattage of lamp $= 40 \times 6 = 240$ watt

Total wattage of tubes $= 125 \times 2 = 250$ watt

Wattage of heater $= 1000$ watt

Thus, the energy consumed by the applicances per day

$$= (240 \times 4) + (250 \times 2) + (1000 \times 3)$$

$$= 4460 \text{ watt-hours}$$

$$= 4.46 \text{ kWh}$$

Thus total energy consumed in 30 days of April month.

$$= 30 \times 4.46 = 133.8 \text{ kWh}$$

Since cost of each unit is 70 paisa = Rs. 0.7

Thus bill for April month is Rs. $= 133.8 \times 0.7 = 93.66$

1.13 SUMMARY

- The movement of free electrons is called electric current or the rate flow of eletcric charge through any conductor material is defined as electric current.
- One ampere is the amount of current which causes one coulomb of charge (equal to 6.25×10^{18} electrones) to pass in one second.
- Average distance covered by free electron between two successive collision is called mean free path of electron.
- The time interval between two successive collision is called relaxation time
- The drift velocity is an average velocity (10^{-4} m/s) with which free electron get drifted towards the positive end of conductor under the influence of an external electric field.
- Resistance is a property of a substances due to which it opposses the flow of electricity through it.
- Law of resistance are summed up as $R=\rho.\frac{1}{A}$ ohm.
- Specific resistance of the material of a conductor is defined as the resistance of unit length and unit area of cross-section of conductor.
- Conductance (G) is reciprocal of resistance (R).
- The emf is not a force but it is energy or work done per unit charge.
- Ohm's law can be written as $R=\frac{V}{I}$. This law is applicable for both AC and DC circuits.
- Equivalent resistance of resistances connected in parallel.

$$\frac{1}{R}=\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}+.....$$

- In a single loop, the current is same at every point.

1.14 REVIEW OF QUESTIONS

Q.1. What is the effect of rise in temperature on the electrical conducitivity of
(i) Metal (ii) Semiconductor (iii) Insulator

Q.2. Define electric power and write its unit.

Q.3. Write expression for equivalent resistance of resistances when
(i) Joined in series (ii) Joined in parallel

Q.4. What do you mean by the resistance of a conductor?

Q.5. Which device is used for increasing or decreasing the current in a circuit?

Q.6. On combining resistances in parallel, total resistance of the circuit decreases or increases.

Q.7. What is the effect of heating a conductor on its resistance?

Q.8. What are the necessary conditions for the validity of Ohm's law.

Q.9. The radius of a wire is reduced to half of its original value by stretching it. What will be its resistance now?

Q.10. Why are resistance wires made from manganin or constantan alloys generally used in resis tance box, standard resistor etc.?

Q.11. Define specifice resistance or resistivity. What are its units? Explain with reasons why:
(a) alloys as manganin and constantan are used to make resistance wires of resistance boxes.
(b) copper wires are used as connecting wire in a circuit.

Q.12. What do you mean by electric current? Define its S.I. unit and mention the direction of electric current in the circuit.

Q.13. Define resistance of a conductor? Explain the factors on which the resistance of conductor depends.

Q.14. State Ohm's law and deduce relation between drift velocity and current of a conductor.

Q.15. Find the total resistance when various resistors are connected
(i) in series (ii) in parallel.

Q.16. What do you understnd by electric power? Write different formula for it.

Q.17. What is meant by specific resistance and conductance of substance? Write their units. Show that electric resistance, of wire depends on resistivity of its material its length and its area of cross-section.

Q.18. A current of 1.6 Amp. is flowing in a conductor? How many electrons pass per second through the conductor?

Q.19. A current 20μA flows in a wire for 30 sec. Calculate (a) the charge flown through the wire (b) the number of electrons flown through the wire.

Q.20. The length of an iron rod is 4 meter and cross-sectional area 2 cm^2. If the specific resistance of iron be 10×10^{-6} ohm–cm. then what will be resistance of rod?

Q.21. Calculate the voltage drop across a 560W resistance when current flowing in it is 20mA.

Q.22. What is the resistance of a lamp, if a 6V battery results in a 100 mA current flow in it.?

Q.23. The resistance of a wire of length 13.78 cm and diameter 0.2 cm is 2.15 ohm. Find the specific resistance of the material of wire.

Q.24. The specific resistance of the material of a wire is 2.62×10^{-8} ohm–meter. If the length of wire is 1.2 m and diameter is 0.04 mm. Find its resistance.

Q.25. Three wires of resistances 10 ohm, 20 ohm and 30 ohm are connected in series and then in parallel. Find the equivalent resistance in each case.

Q.26. Determine the equivalent resistance between the terminals A and B of the network illustrated in Figure (1.15).

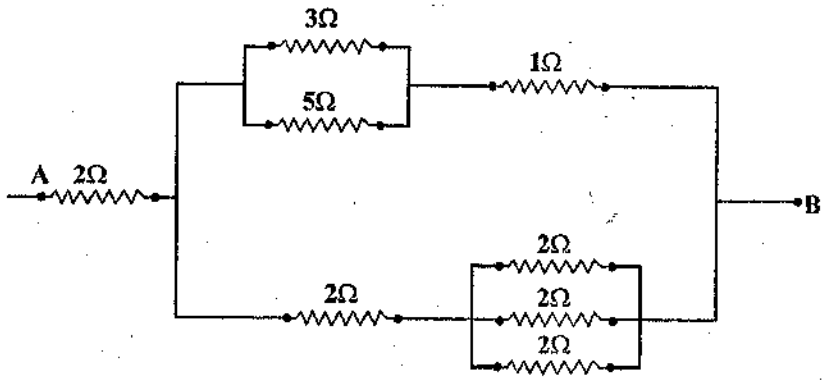


Figure: 1.15

Q.27. What should be the value of R_3 to make the equivalent resistance between A and B equal to R_1?

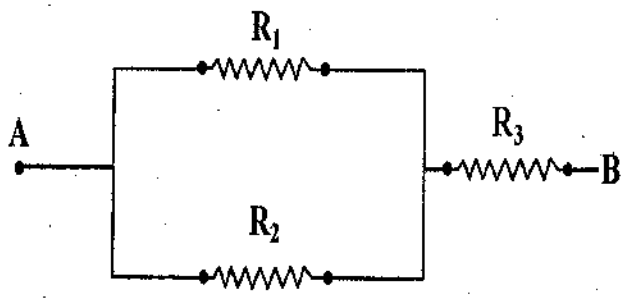


Figure: 1.16

Q.28. Find the equivalent resistance between A and B.

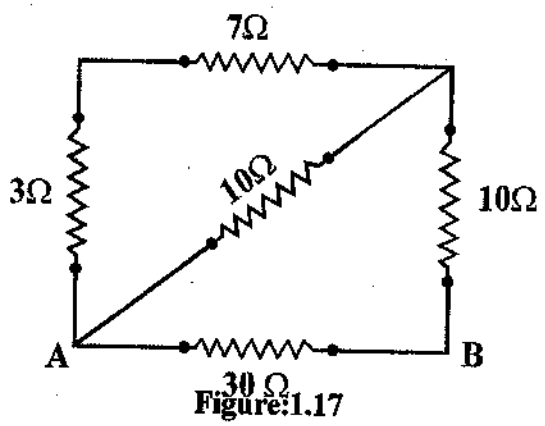


Figure:1.17

Q.29. Five resistances are connected as shown in Figure (1.18). Find the equivalent resistance between A and B.

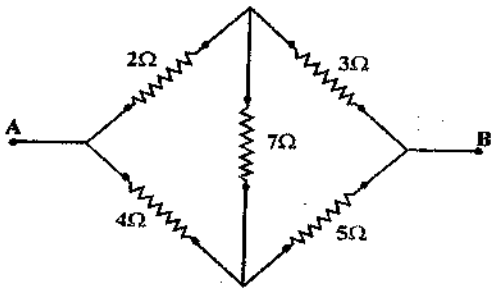


Figure: 1.18

Q.30. Determine the equivalent resistance between the terminals A and B for the network illustrated in Figure (1.19).

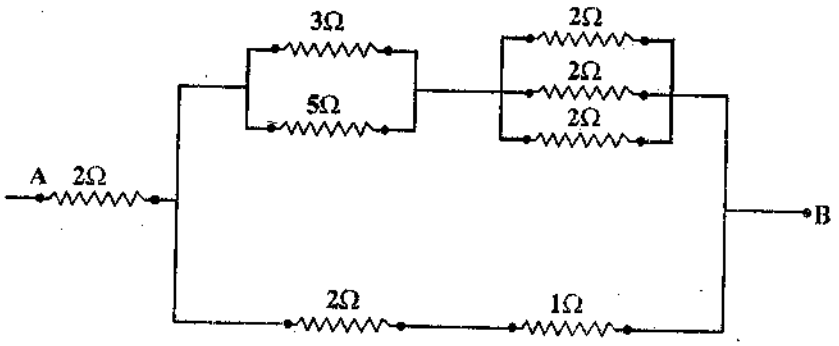


Figure : 1.19

Unit-02
CIRCUITANALYSIS

Content of the Unit

2.0 OBJECTIVE

In this chapter we will discuss–

- How to deal with a complex circuit, namely, multiloop circuit, for which junction rule and loop rule have been given along with illustrative examples.
- The behavior of capacitor while charging and discharging has been studied in details.

2.1 INTRODUCTION OF MULTILOOP CIRCUIT

In general, an electrical ciruit may contain one or more loops each having several branches & junctions. Such a ciruit is called multiloop ciruit. Before taking about multiloop ciruit, it is useful to define two terms, namely, as Junction & Branch. A junction is a point where at least three circuit paths meet and a Branch is a path connecting two junctions. A three loop circuit is shown is Figure (2.1). In this circuit B, C, E & F are junction (nodes) where two or more branches of circuit meet. The part of the circuit through which same amount of current flows everywhere is calles a branch. Thus BAF is one branch and BF, BC, CE & CDE are other branches.

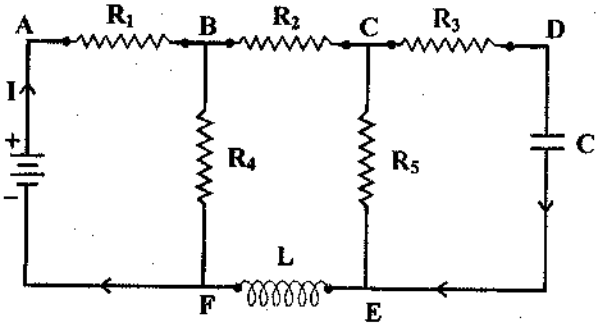


Figure: 2.1

Analysis of multiloop circuits involes the determination of values of current in different branches and potentials at different junction, which is done by following the guidelines known as Kirchoff's Laws.

2.2 KIRCHOFF'S LAWS

As we have learned that simple circuits can be analysed using Ohm's law and rules for series and parallel combination of resistors. The procedure for analyzing multiloop circuits (complex circuits) is simplified by the use of two simple laws called kirchoff's laws.

2.2.1 Kirchoff's First Law (Junction Rule)

According to this, the sum of the currents entering at any junction must be equal to the sum of currents leaving that junction, *i.e.*, the algebraic sum of the currents meeting at any junction or node is zero. This law is also known as *Kirchoof's Current Law* (KCL). The current towards the junction are taken positive and going away from the junction are taken as negative.

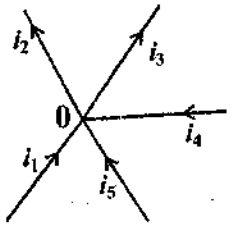


Figure: 2.2

Suppose five conductors meet at O, as shown in Figure (2.2) and currents flowing through these are i_1, i_2, i_3, i_4 and i_5. Currents i_1, i_5 and i_4 are flowing towards the junction and i_2 and i_3 are flowing away from the junction. Thus according to Kirchoff's law

$$i_1 - i_2 - i_3 + i_4 + i_5 = 0$$

$$i_1 + i_4 + i_5 = i_2 + i_3$$

Thus according to this law, if a steady current is flowing in a cirucit, then the charge, does not accumulate at any junction of the circuit, *i.e.*, the rate of flow of charge towards the junction is equal to the rate of flow of charge away from the junction.

Therefore, Kirchoff's first law is equivalent to the law of conservation of charges.

2.2.2 Kirchoff's Second Law (The Loop Rule)

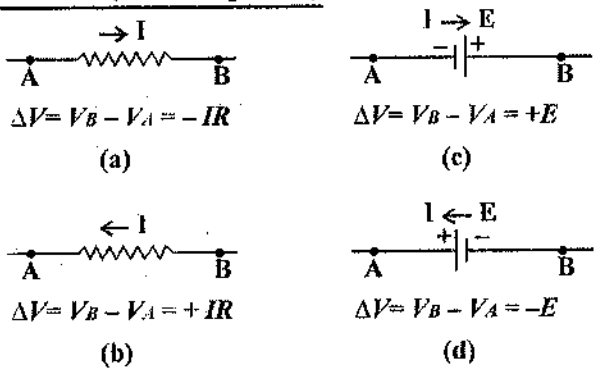


Figure: 2.3

According to this, the sum of potential differences across each elemant around any closed circuit loop mus be zero, *i.e.*, the algebraic sum of the voltages in a specified direction along a closed loop of an electrical circuit is zero. This law is also known as *Kirchoff's Voltage Law* (KVL). As an aid in applying the second rule, the follwing points should be noted.

(i) If a resistor is traversed in the direction of current, the changes in potential accross R is $-IR$ (Figure–2.3a).

(ii) If a resistor is traversed in the direction opposite the current, the changes in potential accross R is IR (Figure 2.3b).

(iii) If a position of e.m.f. is traversed in the direction of e.m.f. (from –ve terminal to +ve terminal) the change in potential is +E.

(iv) If a position of e.m.f. is traversed in the direction opposite to e.m.f. (from +ve terminal to –ve terminal), the change in potential is –E.

Let us understand this law for the Figure (2.4) of resistance network. Battery emf E_1 will be negative as the direction of the current in the battery is from the negative electrode at lower potential to positive electrode at higher potential. Simllarly battery emf E_2 will be positive as the direction of current is in the direction of voltage drop. Thus according to voltage law, starting from point A.

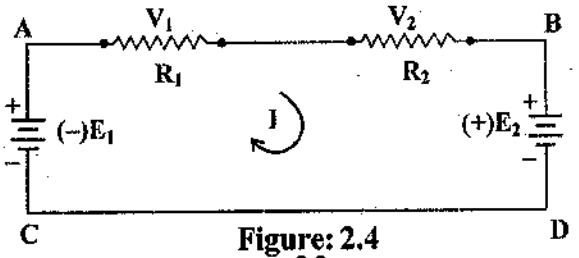


Figure: 2.4

$$V_1 + V_2 + E_2 - E_1 = 0$$

Therefore, $V_1 + V_2 = E_2 - E_1$

The algebric sum of the voltage drops in a closed loop is equal to the sum of e.m.f. in that loop.

Ex.–1 Two cells whose emf and internal resistances are 6V, 0.5 ohm and 10V, 1 ohm are connected in parallel with a resistance of 12 ohm. Calculate the current supplied by each cell.

Solution: Let the current supplied by the cells of emf $E_1 = 6V$ and $E_2 = 10V$ be i_1 and i_2 respectively. From Kirchhoffs first law the current flowing through the resistance of 12 ohm will be $(i_1 + i_2)$. Each cells behaves like a source of emf connected in series with its internal resistance.
Applying Kirchhoffs second law for the closed loop ACDBA

$$i_1 \times 0.5 + (i_1 + i_2) \times 12 = 6$$

$$2.5 i_1 + 12 i_2 = 6 \qquad \text{.....(i)}$$

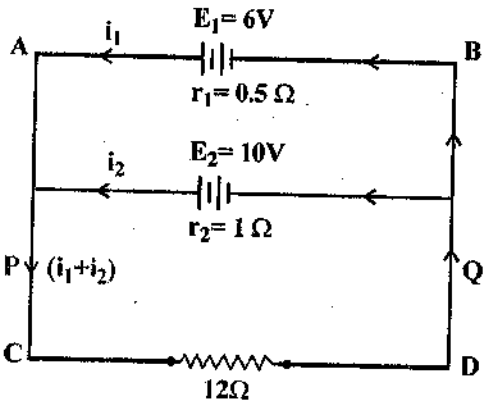


Figure: 2.5

Applying Kirchhoffs second law for the closed loop PCDQP

$$i_2 \times 1 (i_1 + i_2) \times 12 = 10$$

$$12 i_1 \times 13 i_2 = 10 \qquad \text{.....(ii)}$$

Multiplying equation (i) by 13 and equation (ii) by 12

$$162.5 i_1 + 156 i_2 = 78 \qquad \text{....(iii)}$$

$$144 i_1 + 156 i_2 = 120 \qquad \text{....(iv)}$$

Subtracting equation (iv) from equation (iii)

$$\therefore \quad 18.5 i_1 = -42$$

$$\therefore \quad i_1 = -\frac{42}{18.5} = -2.27 \text{ Amp.}$$

Substituting the value of i_1 in equation (ii)

$$-12 \times 2.27 + 13 i_2 = 10$$

$$i_2 = \frac{10 + 27.24}{13} = 2.86 \text{ Amp.}$$

Thus 2.86 Amp. current will be supplied by the cell E_2 and the cell E_1 will get 2.27 Amp. current.

Ex.–2. Calculate the current in each branch of the following circuit.

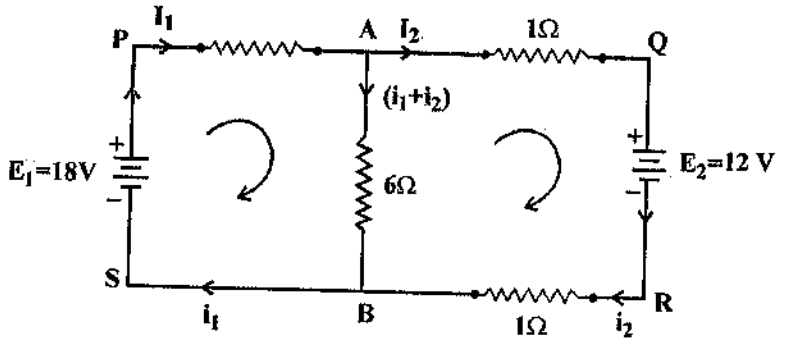


Figure: 2.6

Solution: Suppose the current supplied by the 18V battery is i_1 and by the 12V battery is i_2. According to Kirchhoffs first law at the node A the current flowing through resistance of 6 ohm will be $(i_1 - i_2)$.

Applying voltage law for the closed loop PABSP,

$$i_1 \times 12 + (i_1 - i_2) \times 6 = 18$$

$$2i_1 + (i_1 - i_2) = 3$$

$$3i_1 - i_2 = 3 \qquad \text{.....(i)}$$

Now using voltage law for the closed loop AQRB,

$$i_2 \times 1 + i_2 \times 1 - (i_1 - i_2) \times 6 = 12$$

$$-3i_1 + 4i_2 = 6 \qquad \text{.....(ii)}$$

Adding equations (i) and (ii)

$$i_2 = 3 \text{ Amp.}$$

using the value of i_2 in equation (i)

$$i_1 = 2 \text{ Amp.}$$

$\therefore$ Current flowing through the resistance of 6 ohm.

$$= (i_1 - i_2) = 2 - 3 = -1 \text{ Amp.}$$

Thus 1 Amp. current will flow through the resistance 6 ohm in the direction BA.

Ex.–3. In the given circuit $E_1 = 3V$, $E_2 = 2V$ and $E_3 = 1V$ and $R_1 = R_2 = R_3 = 1$ ohm. Calculate the current flowing through each branch.

Solution: Suppose the currents flowing through the batteries are i_1, i_2 and i_3 as shown in the circuit.

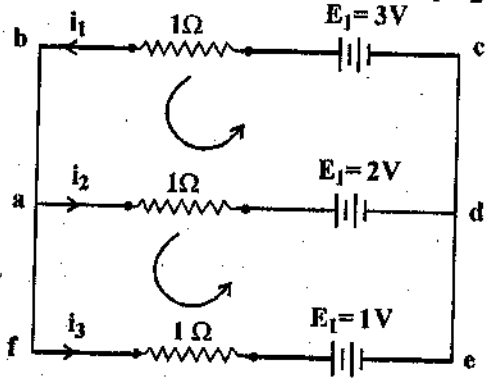


Figure: 2.7

Applying current law at the junction a.

$$i_1 - i_2 - i_3 = 0$$

$$i_3 = (i_1 - i_2) \qquad \text{.....(i)}$$

Applying voltage law in the closed loop badcb.

$$i_1 \times 1 \times i_2 \times 1 = 3 - 2$$

$$i_1 + i_2 = 1 \qquad \text{.....(ii)}$$

Again applying voltage law in the closed loop bfecb.

$$i_1 \times 1 + i_3 \times 1 = 3 - 1$$

$$i_1 + i_3 = 2$$

Using the value of i_3 from equation (i)

$$2i_1 - i_2 = 2 \qquad \text{.....(iii)}$$

Adding equation (ii) and (iii),

$$3i_1 = 3 \qquad i_1 = 1 \text{ Amp.}$$

$\therefore$ From equation (iii), $\qquad i_2 = 0$

and from equation (i),

$$i_3 = (i_1 - i_2) = 1 - 0 = 1 \text{ Amp.}$$

Ex.–4. Using Kirchoff's law to determine the current flowing in $5\,\Omega$ wire in following circuit.

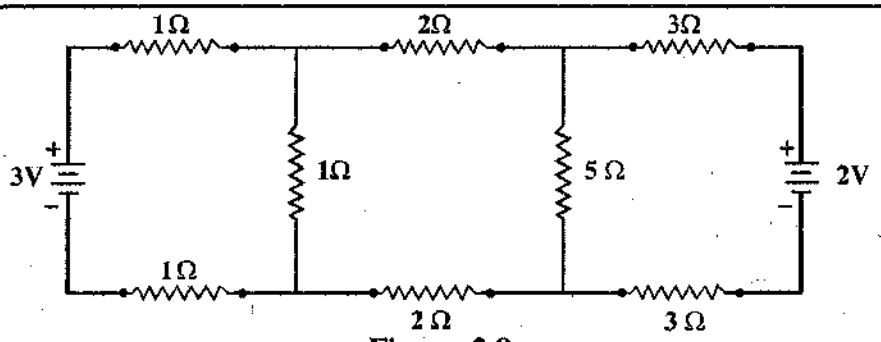


Figure: 2.8

Solution: Let a current i_1 starts from 3V cell and a current i_3 from 2V cell. Thus circuit may redrawn as shown in Figure (2.8).

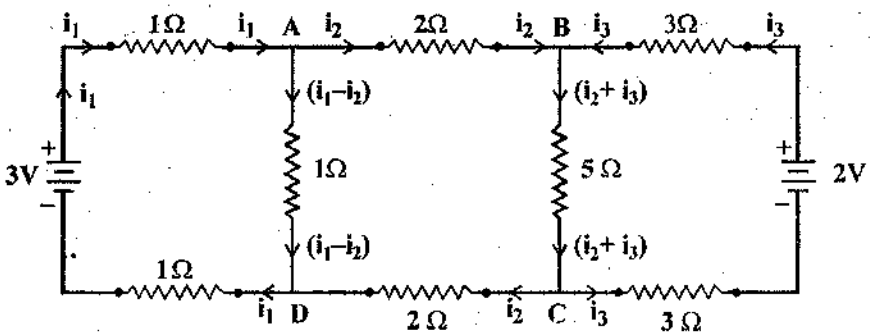


Figure: 2.9

As shown in Figure (2.9), the current i_1 is divided at A in two parts, i_2 flo ws through 2Ω and $(i_1 - i_2)$ through 1Ω. At junctino B, a combined $(i_2 + i_3)$ flow though 5Ω.

Thus, applying Kirchoff's voltage law in Ist mesh.

$$i_1 \times 1 + (i_1 - i_2) \times 1 + i_1 \times 1 = 3$$

$$3i_1 - i_2 = 3 \qquad \text{....(i)}$$

Applying Kirchoff's voltrage law to closed mesh 2

$$i_2 \times 2 + (i_2 + i_3) \times 5 + i_2 \times 2 - (i_1 - i_2) \times 1 = 0$$

$$2i_2 + 5i_2 + 5i_3 + 2i_2 - i_1 + i_2 = 0$$

$$-i_1 + 10i_2 + 5i_3 = 0 \qquad \text{.....(ii)}$$

Applying Kirchoff's voltage law to mesh 3

$$i_3 \times 3 + (i_2 + i_3) \times 5 + i_3 \times 3 = 2$$

or $$5i_2 + 11i_3 = 3$$

Multiplying equation (ii) by 3 and adding to equation (i)

$$-3i_1 + 30i_2 + 15i_3 = 0$$

$$3i_1 - i_2 = 3$$

or solving

$$29i_2 - 15i_3 = 3$$

Multiplying equation (iii) by 15 and (iv) by 11, then solving

$$i_2 = \frac{3}{244} \text{ Amp.}$$

and by putting this value of i_2 in equation (iv)

$$i_3 = \frac{43}{244} \text{ Amp.}$$

The current flowing through $5\,\Omega$ wire is

$$= i_2 + i_3 = \frac{3}{244} + \frac{43}{244} = \frac{46}{244} \text{ Amp.}$$

2.3 CHARGING AND DISCHARGING OF A CAPACITOR

Before we deal the phenomena of charging and discharging of a capacitor. Let's talk in brief about capacitor. Capacitor are commonly used in a variety of electrical circuits.For example, they are used, (i) in tuning the frequency of radio receivers, (ii) as filters in power supplies (iii) to eliminate sparking in automobile ignition system and (iv) as energy storage device in electronic flashing units.

A capacitors basically consists of two conductors carrying equal but opposite charges. The ability of a capacitor to hold charges is measured by a quantity called capacitance. The capacitance depends on the geometry of capacitor and on the metarial seperating the charge conductor, called di-electirc (on insulating material).

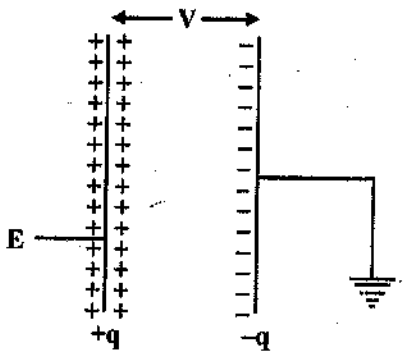


Figure: 2.10

If the charges on plates of a capacitor are +q and -q (by induction) and the potential difference between them is V then capacity of capacitor is given by–

$$C = \frac{q}{V}$$

Where capacitor of capacitor depends on:

(i) Area of plates (A), *i.e.* $C \propto A$

(ii) Distance between plates (d); i.e., $C \propto \frac{1}{d}$

(iii) Medium between plates, i.e., $C \propto E$ (permittivity)

The **SI unit** of capacitance is **Farad.**

Consider a circuit containing capacitor, in which currents vary in time. When a potential difference is applied across a capacitor, the rate at which it charges up depends on its capacitance and on the resistance in the circuit. The charge on the cpacitor increases from zero to maximum value in a finite time similarly, when a charged capacitor is allowed to discharge through a resistance, the charge on the capacitor decreases from maximum value to zero in a finite time. In both cases the time taken to reach the steady state depends on the value of C and R.

2.3.1 Charging of a Capacitor

Suppose a capacitor of capacitance *C*, resistance *R* and a key are connected in series with a battery of emf *E*. Let *q* be the charge on the capacitor at time *t* and *I* be the current in the circuit. Thus the potential difference across the capacitor will be $\frac{q}{C}$.

Using kirchoff's second law

E = Voltage across capacitor + voltage drop across is *r*

$$= \frac{q}{C} + RI \qquad .....(8)$$

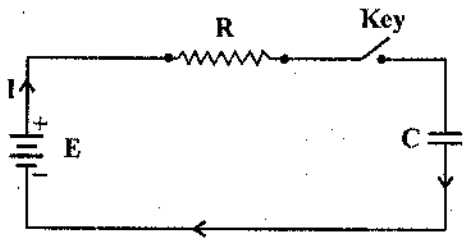


Figure: 2.11

As the time increases, the charge on the capacitor in creases and it finally reaches to maximum value q_0. At the steady state, the potential difference across the capacitor becomes equal to the emf E and the current I reduces to zero.

$$\therefore \qquad E = \frac{q_0}{C} \qquad .....(9)$$

From equation (8) and (9)

$$\frac{q_0}{C} = \frac{q}{C} + RI$$

$$(q_0 - q) = RIC$$

$$\therefore \qquad I = \frac{(q_0 - q)}{RC} \qquad .... (10)$$

by the definetion of current

$$I = \frac{dq}{dt}$$

$$\frac{dq}{dt} = \frac{1}{RC}(q_0 - q) = -\frac{(q - q_0)}{RC}$$

$$\frac{dq}{(q-q_0)} = -\frac{1}{RC}dt$$

integrating on both sides.

$$\int \frac{1}{(q-q_0)} dq = -\frac{1}{RC}\int dt$$

$$\ln(q-q_0) = -\frac{1}{RC}t + \text{const.}$$

But at $t = 0, q = 0$

$\therefore$ $\text{const} = \ln(-q_0)$

$\therefore$ $\ln(q-q_0) = -\frac{1}{RC}t + \ln(-q_0)$

$\Rightarrow$ $\ln(q-q_0) - \ln(-q_0) = -\frac{1}{RC}t$

$\Rightarrow$ $\ln\left(\frac{q-q_0}{-q_0}\right) = -\frac{t}{RC}$

$\Rightarrow$ $\frac{q-q_0}{-q_0} = -e^{\frac{t}{RC}}$

$\Rightarrow$ $\frac{q-q_0}{-q_0} = -e^{-t/RC}$

$\Rightarrow$ $q - q_0 = -q_0 e^{-t/RC}$

$\Rightarrow$ $q = q_0(1 - e^{-t/RC})$ ....(11)

Equation (11) shows that the charge q on the capacitor in increase with time 't' to the maximum values q_0. The variation of q with respect to time t is shown in Figure (2.12).

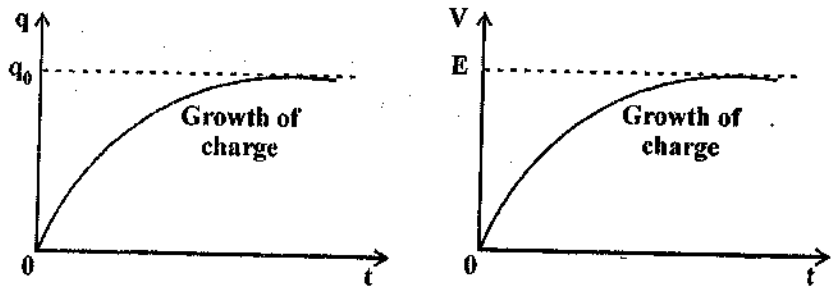


Figure: 2.12

The potential difference across the capacitor $V = q/C$ also increases with time as shown in Figure (2.12).

$$V = \frac{q_0}{C}(1 - e^{-t/RC})$$

$$V = E\,(1 - e^{-t/RC}) \quad \text{.....(12)}$$

where $E = \frac{q_0}{C}$

The current in the circuit I at time t is

$$I=\frac{dq}{dt}=\frac{d}{dt}\{q_0(1-e^{\frac{-t}{RC}})\}]$$

$$I=\frac{q_0}{RC}.e^{-t/RC} \qquad .....(13)$$

where $I_0=\frac{q_0}{RC}$ is the max. value of current at $t=0$.

Thus current dcreases from the maximum value I_0 to zero exponetially with time as shown in Figure (2.13).

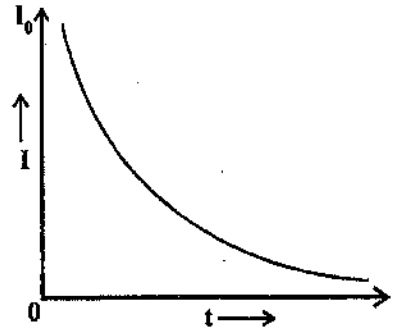


Figure: 2.13

2.3.2 Discharging of a Capacitor

Consider the circuit shown in Figure (2.14). Where a capacitor C is charged to emf E by closing key K_1, while key K_2 is open. Then it is discharged through a resistance R by closing key K_2 (keeping K_1 open). Let q be the charge on the capacitor at the time t and I be the current flowing through R. The initial charge on the capcitor $q_0 = EC$.

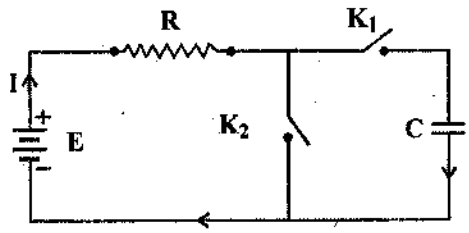


Figure: 2.14

During discharging process, (E = 0), by Kirchoff's voltage law from equation (8),

$$\frac{q}{c}+IR=o.$$

$$\Rightarrow \quad \frac{q}{C}+\frac{dq}{dt}R=0$$

$$\Rightarrow \quad \frac{dq}{dt}=-\frac{q}{RC} \qquad .....(14)$$

Integrating equation (14), we get

$$\ln q=-\frac{t}{RC}+\text{const.}$$

At $t=0$, $q=q_0=EC$

Constant $\ln(q_0)$

On substituting the value of constant–

$$\ln q = -\frac{t}{RC} + \ln q_0$$

$$\Rightarrow \quad \ln q - \ln q_0 = -\frac{t}{RC}$$

$$\Rightarrow \quad \ln\left(\frac{q}{q_0}\right) = -\frac{t}{RC}$$

$$q = q_0 e^{-t/RC} \qquad \text{....(15)}$$

Thus the charges decreases exponentially with time t as shown in Figure (2.15).

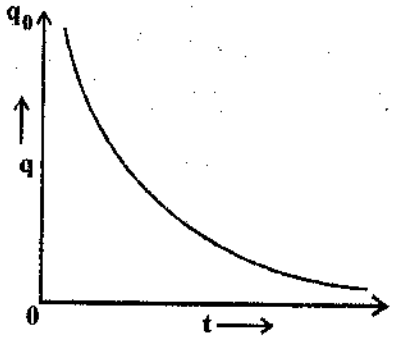


Figure: 2.15

The voltage across the capacitor

$$V = \frac{q}{C} = \frac{q_0}{C} e^{-t/RC} = E e^{-t/RC}$$

Thus voltage also decreases exponentially with time t from the initial value E. as shown in Figure (2.16).

The current in the circuit is

$$I = \frac{dq}{dt} = \frac{d}{dt}(q_0 e^{-t/RC})$$

$$I = \frac{-q_0}{RC} . e^{-t/RC} = -\frac{E}{R} e^{-t/RC}$$

$$I = -I_0 e^{-t/RC} \qquad \text{.....(17)}$$

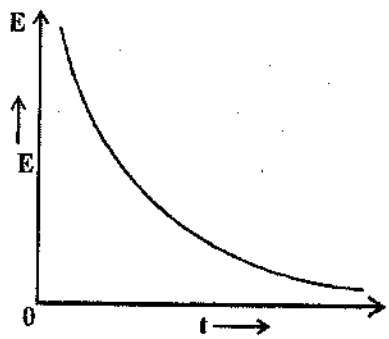


Figure:2.16

Where at $t = 0$ max. current $I = -E/R$ in opposite direction, compared to the charging process. The current then dicreases exponentially

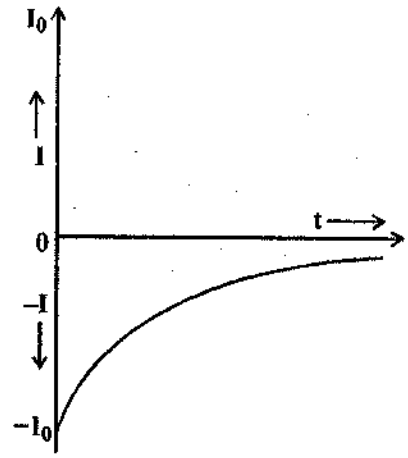


Figure: 2.17

2.4 TIME–CONSTANT OF AN RC CIRCUIT

In an R-C Circuit, the growth of charge and potential difference across the capacitor during charging or decay of charge and potential during discharging are dependent on time. In both processes maximum current flow at start then decays exponentially with time. Thus, the rate of variation of all these quantities depends on the time relative to product RC. The dimension of RC has time and is called *time constant* of circuit denoted by τ .

During charging process, we have

$$q = q(1 - e^{-t/C}),$$

$$V = E(1 - e^{-t/C}),$$

and $$I = I_0 e^{-t/C},$$

and during discharging process

$$q = q_0 e^{-t/C}$$

$$V = E e^{-t/C}$$

$$I = -I_0 e^{-t/C}$$

Therefore at $t = C$, during charging

$$q = q_0(1 - e^{-1}) = q_0(1 - 0.37) \approx 0.63 q_0$$

$$V = 0.63 E$$

$$I = 0.37 I_0$$

and during discharging

$$q = 0.37 q_0$$

$$V = 0.37 E$$

$$I = 0.37 I_0$$

i.e., time constant is the time at which charge, potential on capacitor increases to about 63% to the max. value while current decreases to 37% of the max. value during charging whereas in discharging process, the charge, potential and current decreases to about 37% of the max. values is the time constant (τ).

For larger and smaller values of $\tau = RC$, the variation of q with time are shown in Figure (2.18 a) and (2.18 b) for charging and discharging process respectively.

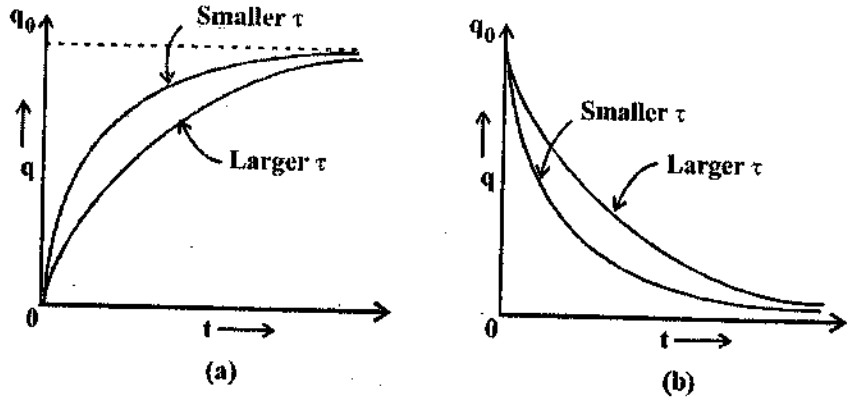


Figure: 2.18

Ex.–5. A 10μF capacitor and 2MW resistor are in series and connected to a 100 V battery. find the time after which charge on capacitor reaches 90% of maximum.

Solution: Given $C=10\mu F=10\times10^{-6}$ F; $R=2M\Omega=2\times10^{6}\Omega$

$$\frac{q}{q_0}=90\%=0.9$$

As $q=q_0(1-e^{-t/CR})$

$$\frac{q}{q_0}=(1-e^{-t/CR})$$

$$0.9=1-e^{-t/CR}$$

$$e^{-t/CR}=0.1$$

$$e^{t/CR}=\frac{1}{0.1}=10$$

$$\frac{t}{CR}=\log_e 10=2.3026$$

$$t=(2.3026)\times CR=2.3026\times10\times10^{-6}\times2\times10^{6}$$

$t=46$ second.

Ex.–6. A 0.18 μF capacitor is first charged and then discharged through a high resistance. If it takes 0.5 sec. for the charge to reduce to one fourth of its initial value. Calculate value of resistance. ($\log_e 4=1.386$).

Solution: Given data $C=0.18\mu F=0.18\times10^{-6}$ F, $t=0.5$ sec.

$$\frac{q}{q_0}=\frac{1}{4}$$

$$q=q_0e^{-t/CR}$$

$$\frac{q}{q_0}=e^{-t/CR}$$

$$\frac{1}{4}=e^{-0.5/0.18\times10^{-6}\times R}$$

$$e^{0.5/0.18\times10^{-6}\times R}=4$$

$$\frac{0.5}{(0.18\times10^{-6})\times R}=\log_e 4=1.386$$

$$R=\frac{0.5}{018\times10^{-6}\times1.386}=2.0\times10^{6}\,\Omega$$

$$R=2\,\text{M}\Omega$$

Ex.7. A capacitor of 4μF is connected to a battery of 24V through a resistance of 0.25 MΩ. Determine the potential difference across the capacitor after 1 second.

Solution: While charging

Charge $q=q_0(1-e^{t/RC})$

Potential difference $V=\frac{q}{C}=\frac{q_0}{C}(1-e^{-t/RC})=E(1-e^{-t/RC})$

Given data $R=0.25\,\text{M}\Omega=0.25\times10^{6}\,\Omega$, $C=4\mu\text{F}=4\times10^{-6}\,\text{F}$

$E=24\,\text{V}$ and $t=1$ sec.

$\tau=RC=0.25\times10^{6}\times4\times10^{-6}=1$ sec.

$\therefore$ $V=24(1-e^{-1/1})=24(1-e^{-1})$

$V=24\times0.63=15$ volts.

2.5 SUMMARY

- The circuit containing more than one loop with their junctions and branches is called multiploop circuits.
- According to Kirchoff's current law, the algebraic sum of currents meeting at a junction is zero.
- Kirchoff's voltage law states that the algebraic sum of electromotive force (emf) and voltage dropp (IR) is zero.
- The equation for charging of a capacitor C through a resistance R is $q=q_0(1-e^{-t/CR})$.
- Growth of charge in charging of capacitor follows an exponential law.
- The equation for discharging of a capacitor C, $q=q_0\,e^{-t/CR}$

2.6 REVIEW OF QUESTIONS

Q.1 What is multiloop circuit?

Q.2 What is the importance of Kirchoff's law?

Q.3 What do you meant by capacitance of a capacitor?

Q.4 Draw graph for growth and decay of charge in a capacitor.

Q.5 State Kirchhoff's laws of current & voltage and explain their application with the help of examples.

Q.6 How does the charging and discharging of a capacitor depends on the resistance con nected in series?

Q.7 What is time constant?

Q.8 A series R–C circuit has a time constant τ. What will be time constant of the circuit shown in Figure (2.19)?

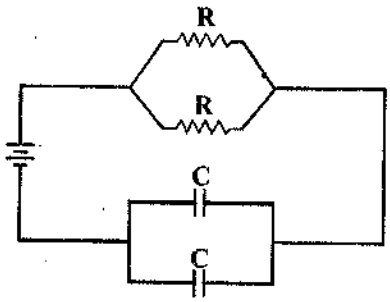


Figure: 2.19

Q.9 Two wires of resistances 30 ohm and 60 ohm are connected in parallel. This combinatino is connected to a voltage source of 30 volt. Determine (i) the total resistance of the circuit, (ii) the current flowing through each resistance.

Q.10 Three resistances of 10 ohm., 15 ohm and 30 ohm are connected in parallel and then con nected to a battery of 15 volt. fidn the total current in the circuit and the current in each resistance.

Q.11 What will be the reading in the ammeter connected in the circuit in the Figure (2.20).

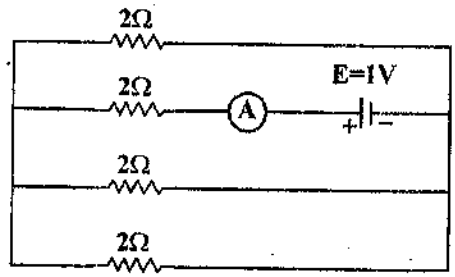


Figure: 2.20

Q.12 How can three resistances of 2, 3, 6 ohm be connected to give an equivalent resistance of 4 ohm.

Q.13 Find the current flowing through the resistances of 5 ohm and 10 ohm in the given circuit.

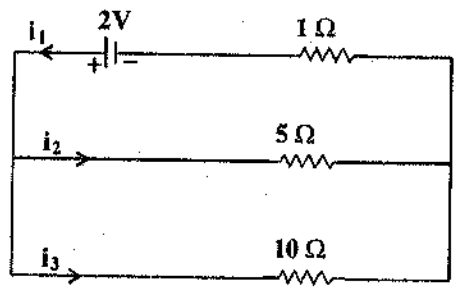


Figure: 2.21

Q.14 How much charge will be stored in the capacitor C connected in the given circuit Internal resistance of the cell is negligible.

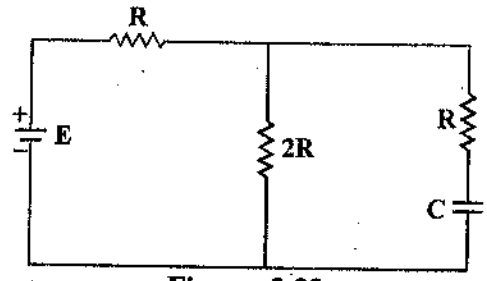


Figure: 2.22

Q.15. Calculate the current in the arm CD of the following cirucit.

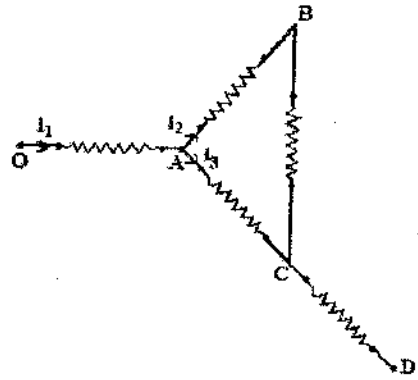


Figure : 2.23

Q.16 Determine the current in the following given circuit.

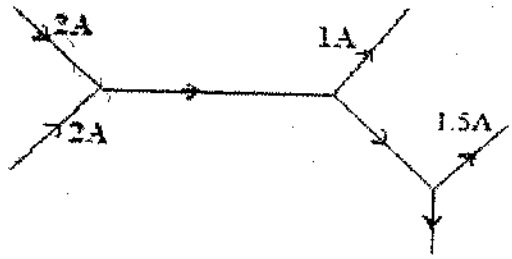


Figure: 2.24

Q.17 In the given resistance circuit, the current flowing through the resistance CD will be:

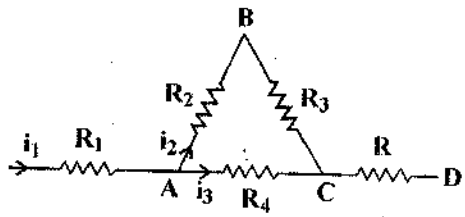


Figure: 2.25

Unit-03
ALTERNATING CURRENT

Content of the Unit

3.0 OBJECTIVE

In this chapter we will discuss–

- The type of currents, namely, direct current (DC) and alternating current (AC).
- Important terminology used in understanding the behaviour of AC.
- Since alternating current has the variation both in magnitude and direction with respect to time, therefore it is interesting to study the circuit containing various elements like resistance(R), capaci tance (C), and inductance (L) or combination of these, which offers different type of resistance,amely impedance, reactance or admittance etc.
- Resonance conditions are also studied for both series and parallel combinations of L,C, and R in a circuit. Power consumed in such circuit.

3.1 INTRODUCTION

The current has been classified broadly in two ways. A.C. (Alternativng Current) and D.C. (Direct Current). In a direct current, the drift velocity superimposed on a random motion of the change carriers (electrons) is in one direction only whereas in an alternating current, the direction of drift velocity changes continuously with a constant time of interval, *i.e.*, usually many time a second.

(i) Direct Current (D.C.):– If the current is obtained from static power supply like cell or battery then it is observed that it constantly flows in a definite directions and its magnitude also remain constant is shown in Figure (3.1) This type of current is called direct current (D.C.) Thus a current whose magnitude remains constant with time and which flows continuously in a definite direction is called direct current.

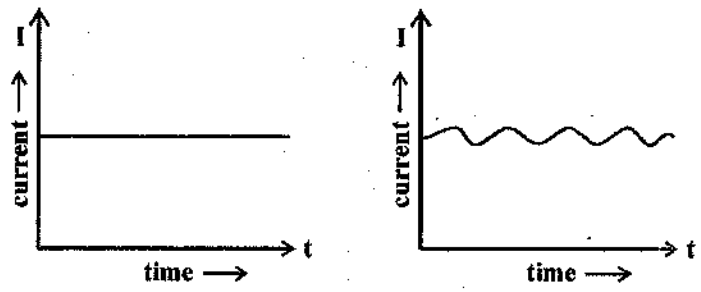


Figure: 3.1

Some time the current is observed such that the direction of current remains constant but the magnitude has small periodic variation with time as shown in Figure (3.1b). Such type of current is called fluctuating direct current. This fluctuating direct current can be visuallized as a composition of a uniform direct current and a periodically working current. The fluctuations in current may have serveral forms and different magnitude for different circuits, which can be removed (rectified) by using a suitable

device called filters (rectifiers) so that the resultant current is almost pure direct current.

(ii) Alternating Current (A.C.): "The current whose directions changes after a definite interval of time is called alternating current". The magnitude of such current changes periodically with time. Such a current can be produced by rotating coil with a definite angular velocity in a uniform magnetic field. The alternating current or voltage can be of many forms according to the wave form as triangular wave, square wave, sinusoidal wave etc.

The simplest and most important alteranting e.m.f. can be represented by a sine curve and is said to be sinusoidal waves form as shown in Figure (3.2).

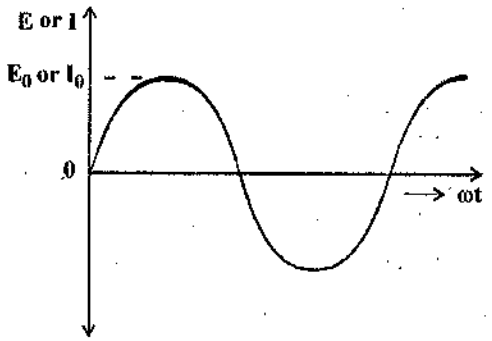


Figure: 3.2

It can be expresed as–

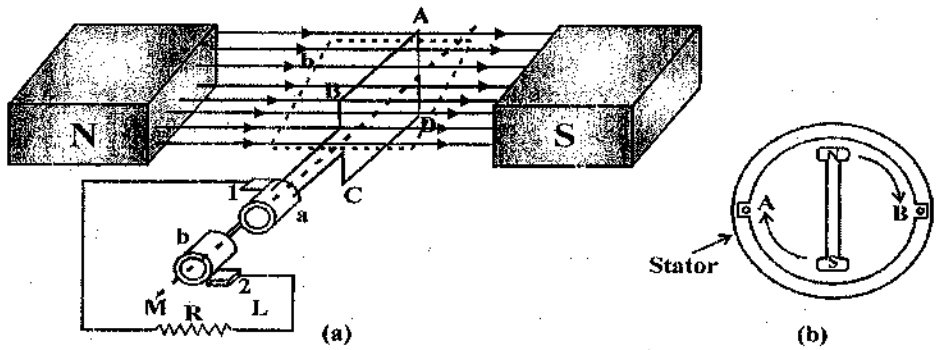
$$E = E_0 \sin \omega t$$

or $$I = I_0 \sin \omega t$$

Where E is the e.m.f. at time t, and E_0, I_0 is the peak value of E or I and ω is constant which is equal to $2\pi f$ where f is the frequency of e.m.f. or I.

3.2 GENERATION OF ALTERNATING E.M.F.

When a coil is placed in an external magnatic field and rotated with a high speed clockwise about a horizontal axis perpendicular to field. Then, the magnetic field linked with the coil changes continuously and an e.m.f. is induced in the coil and if the circuit is closed then an induced current flows in the circuit.



Figrue: 3.3

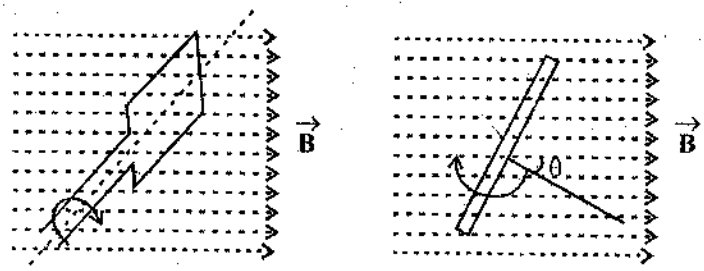
Suppose the coil has n turn and it's area of cross-section (plane) is A. The coil is rotating in a magnatic field B with an angular velocity ω. Suppose, initially the plane of coil is perpendicular to the field then magnetic flux through this coil will be maximum as shown in Figure (3.4a). When the coil is rotated from this position, the magnetic flux starts to change. Suppose, at any time t, coil rotates through an angle θ as shown in Figure (3.4b).

Thus the component of $\vec{B}$ perpendicular to the plane of coil is $B\cos\theta$, then the instantaneous magnetic flux linked with the coil will be

$$\phi = (\vec{B}.\vec{A})n = nBA\cos\theta \qquad \text{.....(1)}$$

where $\theta = \omega t$

$$\therefore \quad \phi = nBA\cos\omega t = \phi_0 \cos\omega t \qquad \text{.....(2)}$$



(a) (b)

Figure: 3.4

Thus according to Faraday's law of electromagnetism the rate of change of magnetic flux will induced the e.m.f. in coil.

$$E = \frac{d\phi}{dt} = nBA\omega\sin\omega t$$

$$E = E_0 \sin\omega t \qquad \text{.....(3)}$$

here $E_0 = nBA\omega$, which is the max. value of induced e.m.f.

If the resistance of the circuit including the coil, i.e. total load is R then.

$$I = \frac{E}{R} = \left(\frac{nBA\omega}{R}\right)\sin\omega r$$

$$I = I_0 \sin\omega r \qquad \text{.....(4)}$$

Thus, it is clear from equation (3) & (4), the induced e.m.f. and current varies periodically with time. Such an e.m.f. and current I are called alternating e.m.f. and current respectively.

(i) when $t = 0, T/2, T, 3T/2, \ldots\ldots$ or $(\theta = 0, \pi, 2\pi, 3\pi, \ldots\ldots)$, i.e., plane of coil is perpendicular to magnetic field $\vec{B}$ then the flux will be maximum $(\phi = \phi_0, -\phi_0)$ but $d\phi/dt$ is minimum so tht induced e.m.f. is minimum. (E or $I = 0$).

(ii) when $t = T/4, 3T/4, 5T/4 \ldots\ldots$ or $(\theta = \pi/2, 3\pi/2, 5\pi/2, \ldots\ldots)$, i.e. the plane of coil is parallel to the magnetic field then the flux will be minimum $(\phi = 0)$ but the $\frac{d\phi}{dt}$ is maximum and the induced e.m.f. or current is maximum $(E_0, -E_0, E_0, -E_0)$, or $(I = I_0, -I_0, I_0, -I_0)$.

Thus it is clear from above, that in first half of the cycle the induced e.m.f. increase from zero to a max. value and then redues to zero. During next half of the cycle, the e.m.f. increase, from zero to a maximum value in the opposite direction and again gradually reduces to zero. Figure (3.7) shows the positions of coil and corresponding induced e.m.f. in the coil.

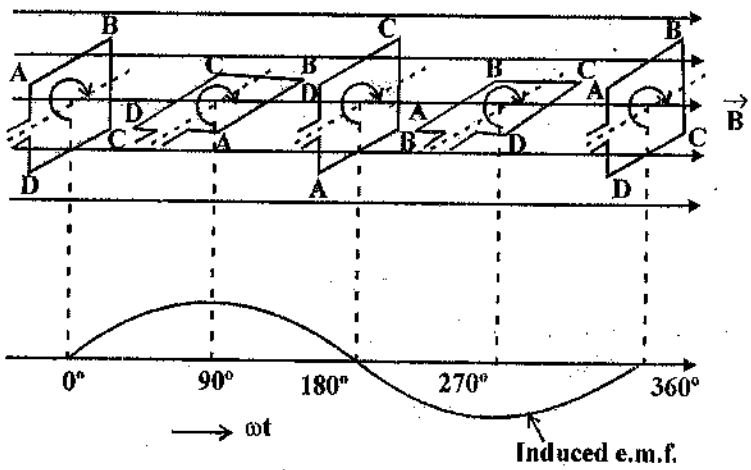


Figure : 3.5

3.3 DIFFERENT TERMINOLOGY RELATED TO ALTERNATING CURRENT OR VOLTAGE

(A) Cycle, Time Period, Frequency, Amplitude, Phase and Phase difference.

(i) Cycle:– One complete set of positive and negative values of an alternating quantitity is known as a cycle, as shown in Figure (3.6).

(ii) Time period:– The time taken by an alternating current to complete one cycle of an alternating quantity is called it's time period. It is designated by T.

$$T = \frac{2\pi}{\omega}$$

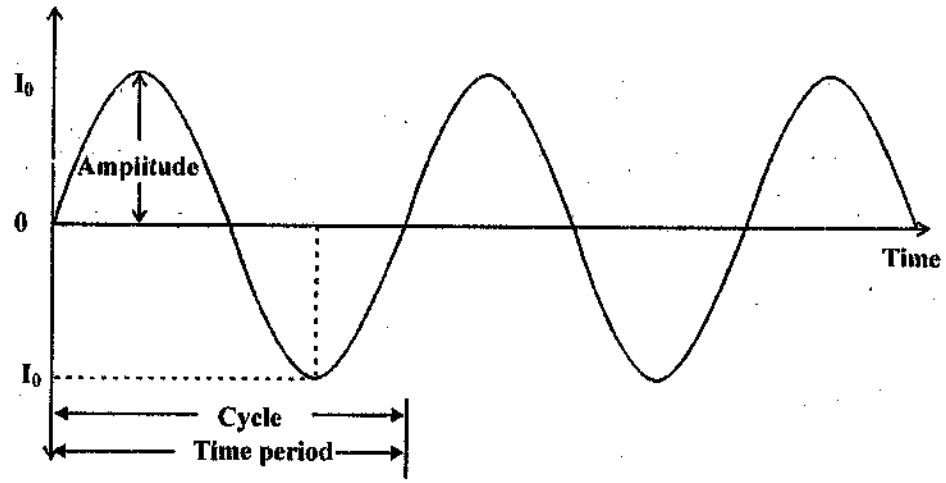


Figure: 3.6

(iii) Frequency:– The number of cycles that occur in one second is called frequency (f) of alternating quantity.

$$f = \frac{\text{Number of cycle}}{\text{Time in second}}$$

$$f = \frac{1}{T} = \frac{\omega}{2\pi}$$

The unit of frequency is hertz (Hz)

(B) Instantaneous, Peak, Average and Root Mean Square Value.

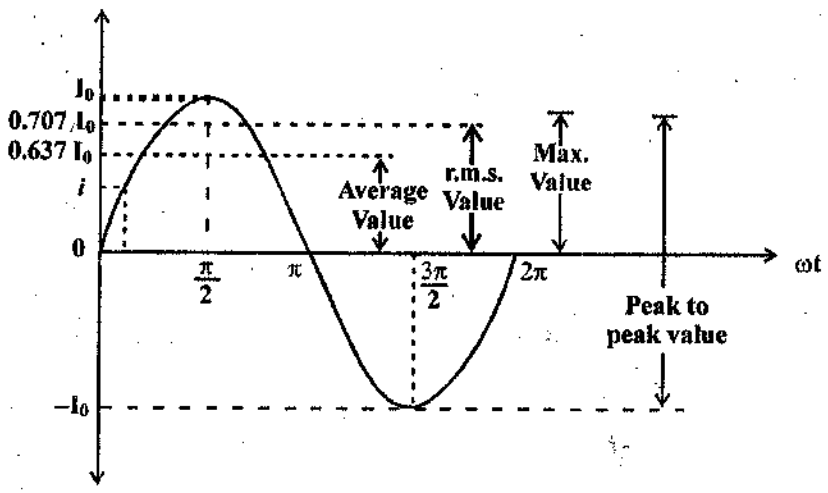


Figure: 3.7

(i) Instantaneous Value:– It any particular time, the value of alternating e.m.f. or current is called instantaneous value. The instanteneous values depend on time and vary simple harmonically in an a.c. circuit. The instantaneous values can be zero.

Instantaneous voltage $E = E_0 \sin \omega t$

Instantaneous current $I = I_0 \sin \omega t$

(ii) Peak Values:– The max. value of current or voltage in a cycle of altenating current or voltage is called peak value. The peak value represents the amplitude of sinusoidal variations. Thus the peak values are E_0 and I_0 respectively. The sum of positive and negative peak values is called peak to peak values.

(iii) Average Value (Mean Value):– Since, the direction and magnitude of alternatign e.m.f. and current change with time thus the average or mean of the instantaneous values over a full cycle is called mean or average value. In a full cycle, the mean value of alternating e.m.f. and current is zero, because the first half of the cycle is positive and other next half cycle is negative. As a result, their sum over full cycle becomes zero so the mean value is zero.

Instantaneous current $I = I_0 \sin \omega t = I_0 \sin \theta$, consider an elementary strip of width $d\theta$ in first half cycle.

Then the area of strip $= I.d\theta$

$\therefore$ Area of half cycle $= \int_0^{\pi} I.d\theta$

$$= \int_0^{\pi} I.d\theta$$

$$= \int_0^{\pi} I_0 \sin\theta \, d\theta = 2I_0$$

$$\therefore \quad \text{Average value} = \frac{\text{Arc of half cycle}}{\text{Base}} = \frac{2I_0}{\pi} = 0.637\, I_0 \quad ...(5)$$

(iv) Root Mean Square Value:– The mean of square of the voltage or current over a full cycle is called mean square value and the square root of the mean square value is called root mean sqyare value. The root mean square value or RMS of e.m.f. is represented by E_{rms} and of current is represented by I_{rms}.

$$E_{rms} = (\bar{E}^2)^{1/2} \qquad .....(7)$$

$$I_{rms} = (\bar{I}^2)^{1/2} \qquad .....(6)$$

The square of instantaneous values of alternating voltage and current are always positive so the rms values are never zero.

Q $\quad E = E_0 \sin\theta$

Square of alternating emf. $E^2 = E_0^2 \sin^2\theta$

Average of the square of alteranting emf over a cycle

$$\bar{E}^2 = \frac{1}{2}\int_0^{2\pi} E_0^2 \sin^2 d\theta$$

$$= \frac{E_0^2}{2\pi}\int_0^{2\pi} \frac{(1-\cos 2\theta)}{2} d\theta$$

$$= \frac{E_0^2}{4\pi}\left[\theta - \frac{\sin 2\theta}{2}\right]_0^{2\pi}$$

$$= \frac{E_0^2}{4\pi}.2\pi = \frac{E_0^2}{2}$$

Hence the root mean square value of the emf is

$$E_{rms} = (\bar{E}^2)^{1/2} = \frac{E_2}{\sqrt{2}} = 0.707\, E_0$$

Similarly, $I_{rms} = 0.707\, I_0$ ....(8)

The root-mean square value of alternating current or voltage are also called virtual values or effective values.

Ex.1 In an AC circuit the rms value of emf. is 220 volts. Determine the peak value.

Solution: $E_{rms} = 200$ Volts, and $E_{rms} = \frac{E_0}{\sqrt{2}}$

$\therefore \quad E_0 = \sqrt{2} \times E_{rms}$

$E_0 = \sqrt{2} \times 220 = 311.08$ volts.

Ex. 2. In an AC circuit the peak value of current is 4.0 ampere. If in the circuit (a) an AC ammeter or (b) DC ammeter are connected, what will be their readings?

Solution: (a) AC ammeter reads the rms value of current, hence its reading will be

$$I_{rms} = \frac{I_0}{\sqrt{2}}$$

$$I_{rms} = \frac{4}{\sqrt{2}} = 2\sqrt{2} = 2.828 = 2.83 \text{ Amp.}$$

(b) The DC ammeter will read the mean value of current and as mean value in AC is zero hence its reading will be zero.

Ex. 3. The alternating voltage applied in a circuit is $E = 200 \sin(314t)$ volts. So that the current is $I = 2 \sin(314t + \pi/3)$ amperes. Calculate the following (a) frequency of applied voltage, (b) rms values of voltage and current.

Solution: (a) Angular frequency of applied voltage $\omega = 314 = 2\pi n$

$\therefore \quad n = \frac{314}{2 \times 3.14} = 50$ Hz.

(b) RMS value $= \frac{\text{Peak Value}}{\sqrt{2}}$

$\therefore$ RMs value of voltage $E_{rms} = \frac{E_0}{\sqrt{2}} = \frac{220}{\sqrt{2}} = 141.4$ Volts.

RMS value of current $I_{rms} = \frac{I_0}{\sqrt{2}} = \frac{2}{\sqrt{2}} = 1.414$ Ampere

Ex. 4. What is peak value of an alteranting current which produces three times the heat per second as direct current of 2.0 Amp. in a resistor R?

Solution: Heat per second by $2A = 1^2 R = 2^2 R = 4R$

Three times heat per second $= 3 \times 4R = 12R$

If I_r is the r.m.s. value of the AC, heat per seocnd is $R = I_r^2 R$

So $I_r^2 R = 12R$ and $I_r^2 = 12$

So r.m.s. value $(12)^{1/2}$

peak value $=(2)^{1/2}\times r.m.s.$

$$=(2)^{1/2}\times(12)^{1/2}=(24)^{1/2}=4.9\,\text{Amp.}$$

Ex. 5. An AC of frequncy 50 Hz has maximum value of 10 amperes. In how much time till it reach a value of 7 amperes for the first time starting from the zero value? What is the r.m.s. value?

Solution: We have $I=I_0\sin\omega t$

$$\omega=2\pi f=2\pi\times50=100\pi$$

Let it reach the required value in t seconds; then

$$7=10\sin100\pi t$$

So $\sin100\pi t=7/10=0.7$

$\therefore$ $100\pi t=44.4^\circ=\pi(\pi/180)\times44.4$ radians

This gives $t=\dfrac{44.4}{180\times100}=0.0024$ sec.

$$I_{rms}=\frac{I_0}{\sqrt{2}}=0.707\,I_0=0.707\times10;$$

$$I_{rms}=7.07$$

Ex. 6. The frequency of an alternating voltage is 50 cycle/sec and its amplitutde is 100 volt. Show complete three cycles in time voltage graphs and calculate itsl root mean square value.

Solution: Given $f=50$

$\therefore$ Periodic time $=\dfrac{1}{50}=0.02\,\text{sec.}$

and $V_0=100$ volt.

Hence, time-voltage graph is shown as Figure (3.22).

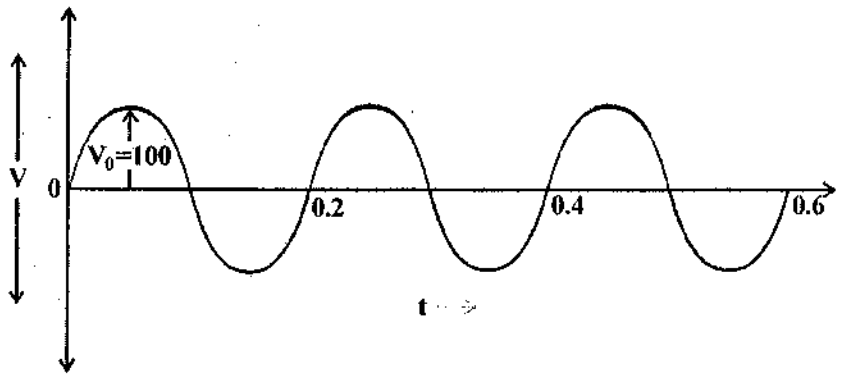


Figure: 3.8

Now $V_{rms}=\dfrac{V_0}{\sqrt{2}}$

$$V_{rms}=0.707\,V_0=0.707\times100=70.7\,\text{Volts.}$$

3.4 ANALYSIS OF AC CIRCUIT

The closed path followed by alternating current is called an AC circuit. When a sinusoidal alternating

volltage is applied in a circuit, the resulting current is also sinusoidal and has the same freqnency as applied voltage. However, there is a phase difference between applied voltagte and resulting current. In a circuit, the phase difference θ depends upon the nature of circuit.

The circuit, elements of an alternating current circuit are resistance, inductance, resistance, capacitance. When alternating current flow through these elements the e.m.f. applied and the resulting current donot remain in phase. In some ac circuits, the current become maximum after the maximum of e.m.f. then the pase of current is behind the e.m.f. and inother case, when current gains maximum value before the e.m.f. becomes maximum then e.m.f. lags behind the current. We will now consider different ac circuits and study the phase relationship between them.

(A) AC Circuit Containing Resistance only

Suppose a circuit containing resistance R connected to alternating e.m.f. source E as shown in Figure (3.9).

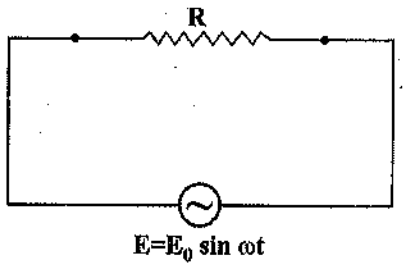


Figure : 3.9

$$E = E_0 \sin \omega t \qquad .....(9)$$

According to Ohm's law

$$I = \frac{E}{R} = \frac{E_0}{R} \sin \omega t \qquad .....(10)$$

$$I = I_0 \sin \omega t$$

Thus it is clear from equation (9) and (10), the alternating e.m.f. and current one always remains in phas ewith each other as shown in Figure (3.10).

The ratio E / I or E_o / I_0 is called impedance (resitance) R of circuit.

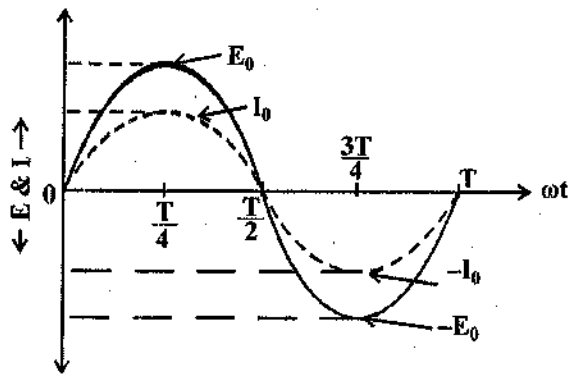


Figure:3.10

(B) AC Circuit Containing Pure Inductance only

Suppose a coil is connected to a source of a laternating e.m.f. in a ac circuit. The coil has an inductance L with negligible resistance.

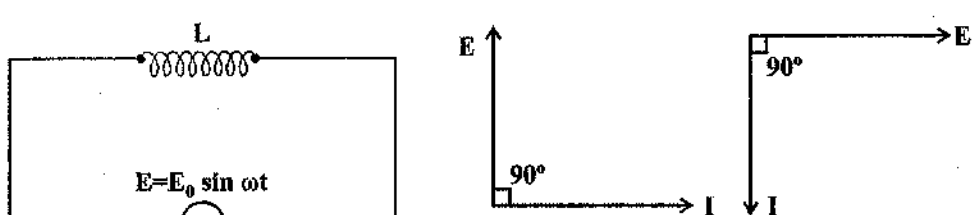


Figure: 3.11

The e.m.f. at time 't' is given by–

$$E = E_0 \sin \omega t \qquad \text{.....(11)}$$

Due to this e.m.f. an alternating current flows and hence an induced e.m.f. is produced due to self induction, which opposes the changes in the current altenery steps, is given by

$$e = -L\frac{dI}{dt} \qquad \text{..... (12)}$$

Since there is no other Ohmic elements in the circuit, which may cause drop of potential. Therefore the total e.m.f. in the circuit will be equal to the drop of potential in the circuit, i.e.

$$E = L\frac{dI}{dt}$$

$$\Rightarrow \quad L\frac{dI}{dt} = E_0 \sin \omega t$$

on integrating both sides

$$\int I = \frac{E_0}{L}\int \sin \omega t \, dt$$

$$\int I = \frac{-E_0}{\omega L}\cos \omega t = -I_0 \cos \omega t$$

where $I_0 = \dfrac{E_0}{\omega L}$

$$\Rightarrow \qquad I = I_0 \sin(\omega t - \pi/2) \qquad \text{.....(14)}$$

Comparison of equation (13) and (14) reveals that the phase of current at time t will be $(\omega t - \pi/2)$ while the of e.m.f. will be ωt. Thus the current lags behind e.m.f by a phase angle of $\pi/2$ or 90°. when e.m.f. achieved max. value then the current zero and vice-versa.

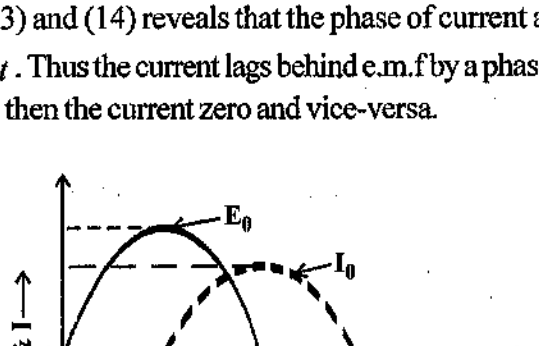


Figure: 3.12

The ratio E/I or E_0 / I_0 is resistance of circuit. Since this resistance is only due to inductance, it is called "inductive reactance" and is represented by X_L.

$$X_L = \omega L = 2\pi f L \qquad \text{.....(15)}$$

(C) AC Ciruit Containing Capacitance only

Suppose an ac circuit contains a capacitor of capacitance C connected across an alternating supply of e.m.f.

$$E = E_0 \sin \omega t \qquad \text{.....(16)}$$

Suppose at certain time 't' the change on the conduenser is q and thus the potential difference across it will be $V = q/C$. This potential difference will be equal to the applied alternating e.m.f. at that time, *i.e.*

$$V = \frac{q}{C} = E \quad \Rightarrow \frac{q}{C} = E_0 \sin \omega t \Rightarrow \; q = CE_0 \sin \omega t \qquad \text{.....(17)}$$

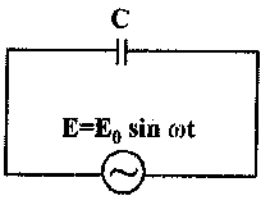


Figure: 3.13

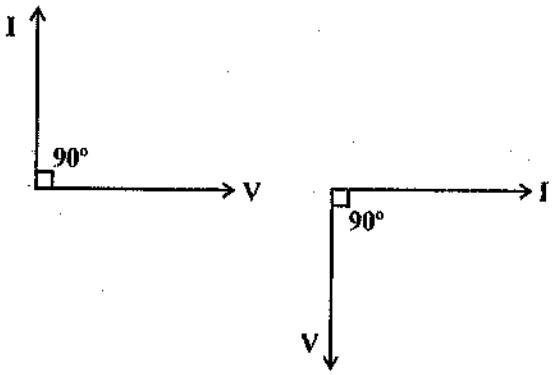


Figure: 3.14

But the rate flow of charge is current. Therefore

$$I = \frac{dq}{dt} = \frac{d}{dt}(CE_0 \sin \omega t) = CE_0 \omega \cos \omega t$$

$$I = C\omega E_0 \sin(\omega t + \pi/2)$$

$$I = I_0 \sin(\omega t + \pi/2) \qquad \text{.....(18)}$$

where $I = I_0 \sin(\omega t + \pi/2)$ where $I_0 = \dfrac{E_0}{1/\omega C}$ is the peak value.

Thus the current in the circuit is alternating and of the same frequency as of the applied e.m.f. On comparing equations for current I and E, it is clear that the phase angle of current is ahead by the phase anlge of e.m.f. by 90°, or in other words e.m.f. (E) lags behind the current by $\pi/2$.

The ratio E/I or E_0 / I_0 is the resistance of circuit. Since this resistance is due to only capacitance C, therefore it is called capacitive reactance and represented by X_C.

i.e., $$X_C = \frac{1}{\omega C} = \frac{1}{2\pi f C} \qquad \text{.....(19)}$$

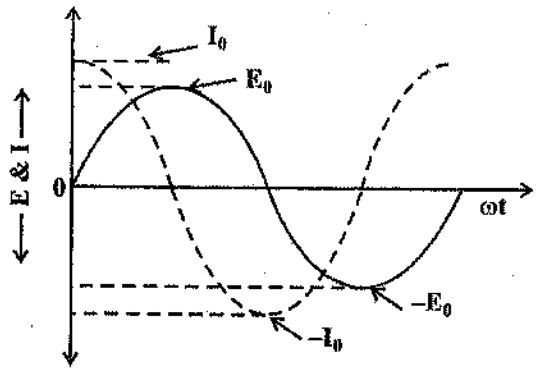


Figure: 3.15

Thus, from (a), (b) and (c) summarizing the facts of phase relationship between voltage drop across the element and current through them is that, in a purely resistive circuit the alternating e.m.f. E and current I are always in phase, in a purely inductive circuit e.m.f. (E) is ahead of current (I) by a phase angle of $\pi/2$ and in purely capacitance circuit, E logs behind the current by $\pi/2$.

(D) AC Circuit Containing Inductance and Resistance in Series

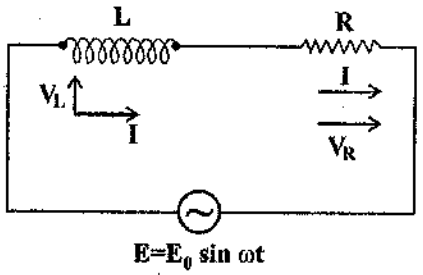


Figure: 3.16

Suppose an inductance L and a resistance R are connected in series to an alternating e.m.f. in series to an alternating e.m.f. $E = E_0 \sin \omega t$ is a circuit. The potential difference across R and L are V_R and V_L respectively.

Since R and L are connected in series therefore the current I will be same in both elements. Let I be current in the circuit at time t.

$$V_R = IR$$

$$V_L = IX_L = I\omega L$$

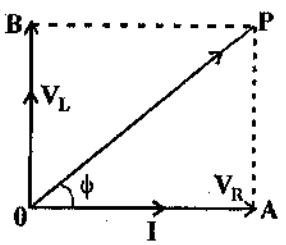


Figure: 3.17

Here the potential drop V_R in phase with current I while the potential drop V_L will be ahead of I by a phase angle of $\pi/2$, as shown in vector diagram.

The resultant of these vector is OP, which represents the voltage across the series combination of R and L and will be equal to the applied voltage E.

Therefore, from vector diagram.

$$OP^2 = OA^2 + AP^2$$

$$E^2 = V_R^2 + V_L^2$$

$$E = \sqrt{(IR)^2 + (IX_L)^2}$$

$$E = I\sqrt{R^2 + X_L^2} = I\sqrt{R^2 + \omega^2 L^2}$$

Applying Ohm's law, the quantity $\sqrt{R^2 + X_L^2}$ offers net resistance to the current flow in the circuit is called "impedance" of the circuit and represented by Z_{RL}. *i.e.*,

$$Z_{RL} = \sqrt{R^2 + X_L^2} = \sqrt{R^2 + \omega^2 L^2} \qquad .....(20)$$

The quantity Z_{RL} measured in Ohm. The reciprocal of impedance is called "Admittance" of the AC circuit. It is measured in Mho.

From phase diagram it is clear that is LR circuit, the current I lags behind the applied voltage E by a phase angle ϕ.

$$\tan\phi = \frac{V_L}{V_R} = \frac{I\omega L}{IR} = \frac{\omega L}{R} \qquad .....(21)$$

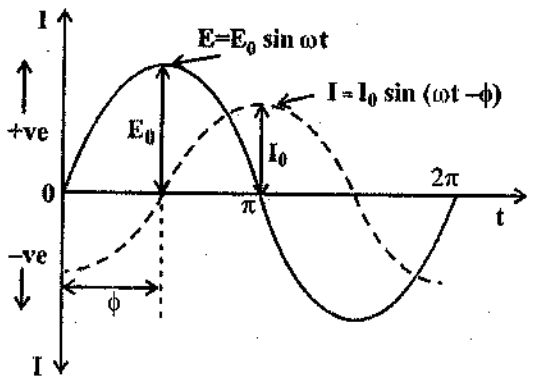


Figure: 3.18

(E) AC Circuit Containing Capacitance (C) and Resistance (R) in series

The analysis is similar but in this case the potential difference across R and C will be V_R and V_C respectively.

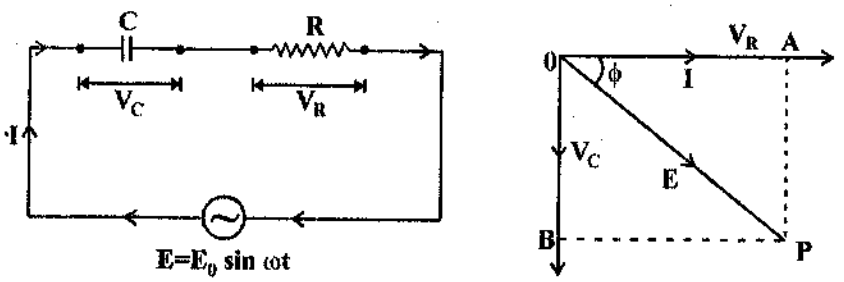


Figure: 3.19

If I is the current in the circuit then

$$V_R = IR$$

$$V_C = IX_C = \frac{I}{\omega C}$$

As it is shown in phase vector diagram, V_R and I will be in same phase while V_C will lag behind I by 90°.

From VOAP

$$OP^2 = AP^2 + OA^2$$

$$E^2 = V_C^2 + V_R^2$$

$$E^2 = I^2R^2 + I^2X_C^2$$

$$E = \sqrt{I^2R^2 + I^2X_C^2} = I\sqrt{R^2 + X_C^2}$$

where $\sqrt{R^2 + X_C^2}$ represents the net resistance of the circuit, called as "Impedance" (Z_{RC}) of the circuit.

$$Z_{RC} = \sqrt{R^2 + X_C^2}$$

$$Z_{RC} = \sqrt{R^2 + \frac{1}{\omega^2 C^2}} \qquad .....(22)$$

(E) AC Circuit Containing Capacitance (C) and Resistance (R) in Series

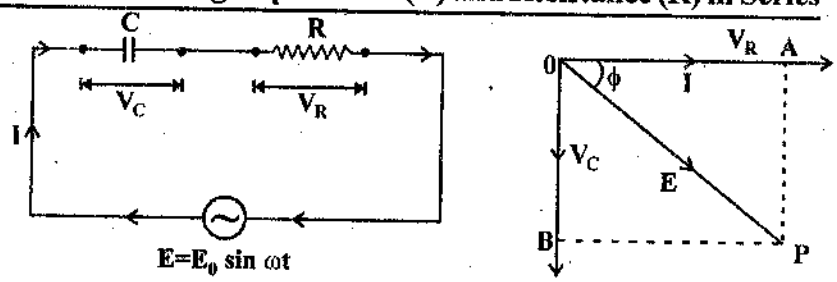


Figure: 3.20

The analysis is similar but in this case the potential difference across R and C will be V_R and V_C respectively.

If I is the current in the circuit then

$$V_R = IR$$

$$V_C = IX_C = \frac{I}{\omega C}$$

As it is shown in phase vector diagram, V_R and I will be same phase while V_C will la g behind I by 90°.

From ΔOAP

$$OP^2 = AP^2 + OA^2$$

$$\Delta E^2 = V_C^2 + V_R^2$$

$$E^2 = I^2R^2 + I^2X_C^2$$

$$E = \sqrt{I^2R^2 + I^2X_C^2}$$

$$E = I\sqrt{R^2 + X_C^2}$$

where $\sqrt{R^2 + X_C^2}$ is repre sents the net resistance of the circuit, called as Impedance (Z_{RC}) of the

circuit.

$$Z = \sqrt{R^2 + X_C^2}$$

$$Z = \sqrt{R^2 + \frac{1}{\omega^2 C^2}}$$

The quantitity Z_{RC} is measured in ohm and its reciprocal is called admittance of the circuit and is measured in mho.

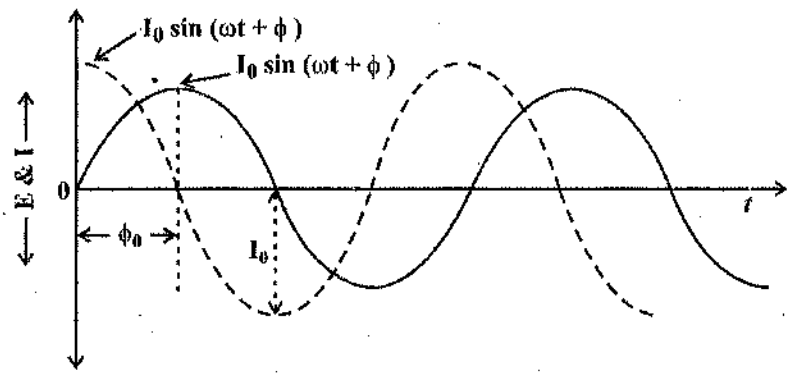


Figure: 3.21

If the phase difference between E and I is ϕ, then from vector phase diagram,

$$\tan\phi = \frac{V_C}{V_R}$$

$$\tan\phi = \frac{I/\omega C}{IR} = \frac{1}{R\omega C} \qquad \text{.....(23)}$$

(F) AC Circuit Containing Inductance L, Capacitance C

In this case, the potential difference across L and C are V_L and V_C respectively, where V_L leads the current I in phase by 90° while V_C lags behind the current I in phase by 90°. Therefore, the total phase difference between V_L and V_C are 180°, i.e., they are in opposite phase each other.

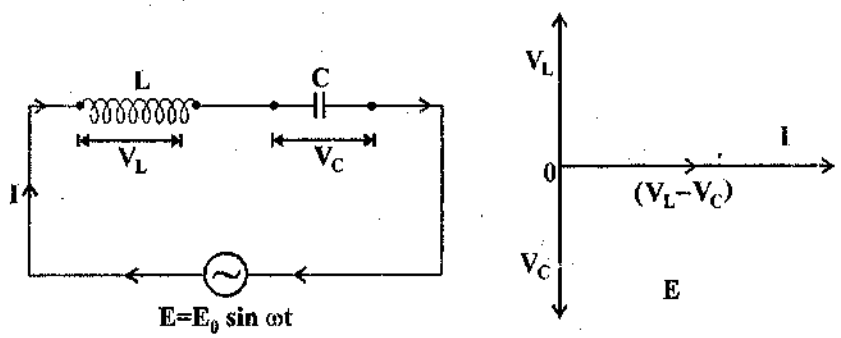


Figure: 3.22

Thus, the net potential difference in $(V_L - V_C)$ which should be equal to the applied emf.

$$E = V_L - V_C$$

and also the net impedance of circuit is

$$Z_{LC} = X_L - X_C$$

$$Z_{LC} = \omega L - \frac{1}{\omega C} \qquad \text{.....(24)}$$

If $X_L = X_C$, than $Z_{LC} = 0$ i.e. net resistance (impedance) offered by the circuit is zero and amplitude of current will be finite. This situation is known as *"Electrical Resonance"*.
Thus, for electrical resonance

$$X_L = X_C$$

$$\omega L = \frac{1}{\omega C}$$

$$2\pi f L = \frac{1}{2\pi f L}$$

$$f^2 = \frac{1}{4\pi^2 LC}$$

$$f = \frac{1}{2\pi\sqrt{LC}} \qquad \text{....(25)}$$

This frequency is known as resonant frequency of the circuit.

(G) AC Circuit Contaning Inductance (L), Capacitance (C), and Resistance (R) in series

Suppose an inductance (L), capacitor of capacitance (C) a resistance R are joined in series and connected to an applied emf source $E = E_0 \sin \omega t$, as shown in Figure (3.22). It is clear from phasor diagram (3.22 b) that V_L leads the current vector I by 90° V_C lags behind by 90° and V_R is in phase with it. V_L and V_C are therefore 180° out of phase i.e. in antiphase. If V_L is greater than V_C, their resultant $(V_L - V_C)$ is in the direction of V_L. Thus, the vector sum of $(V_L - V_C)$ and R equals the applied emf E, therefore.

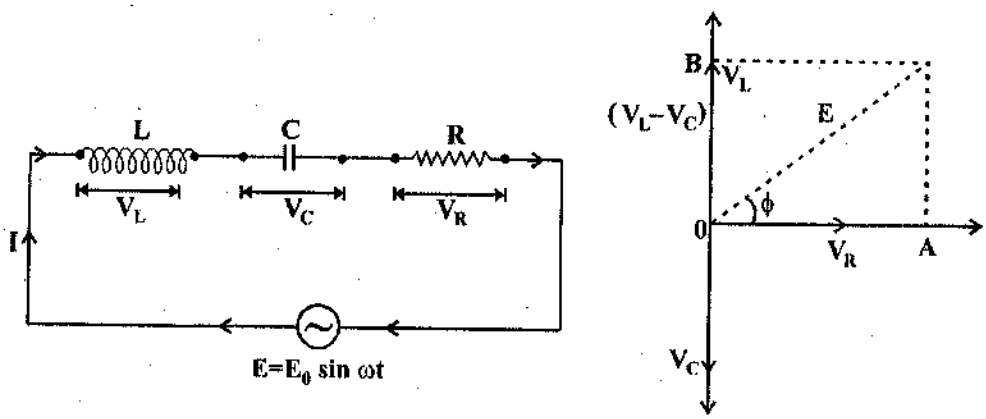


Figure: 3.23

$$E^2 = V_R^2 + (V_L - V_C)^2 \qquad \text{.....(26)}$$

It the net resistance (impedance) of the series combination is Z than $E = IZ$.

$$\therefore \quad (IZ)^2 = I^2R^2 + (IX_L - IX_C)^2$$

$$Z^2 = R^2 + (X_L - X_C)^2$$

$$Z = \sqrt{R^2 + (X_L - X_C)^2}$$

Puttig the valuesof X_L a X_C, we get

$$Z = \left[R^2 + \left(\omega L - \frac{1}{\omega C} \right)^2 \right]^{1/2} \qquad \text{.....(27)}$$

From phase diagram, it is noted that applied emf E leads the current I by a phase angle of ϕ, i.e.

$$\therefore \quad \tan\phi = \frac{V_L - V_C}{V_R} = \frac{X_L - X_C}{R}$$

$$\tan\phi = \frac{\omega L - \frac{1}{\omega C}}{R} \qquad \text{.....(28)}$$

Now, we consider three different situations.

Case I: If $\omega L > \frac{1}{\omega C}$, then the phase angle ϕ will be positive and the resultant voltage will lead the current I. The circuit will be inductive in nature.

Case II: If $\omega L < \frac{1}{\omega C}$, then phase angle ϕ will be negative and voltage will lag behind the current in phase. The cirucit will be capacitive in nature.

Case III: If $\omega L = \frac{1}{\omega C}$, then phase angle ϕ will be zero and the voltage and current will be in same phase. This condition is called "Resonance". In this case impedance of the circuit is minimum (Z=R) and thus circuit will now be purely resistance.

Resonance in LCR Series Circuit

At resonant frequency $\omega = \omega_0$, the inductive reactance X_L and capacitive reactance X_C becomes equal. Therefore

$$X_L = X_C; \qquad \omega_0 L = \frac{1}{\omega_0 C}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad \text{or} \quad f_0 = \frac{1}{2\pi\sqrt{LC}} \text{ Hz.}$$

The following pecularities are observed at resonance:

(i) The impedance of the circuit is minimum and it is totally equal to the resistance of the circuit

$$Z = Z_{min} = R$$

(ii) The applied emf and resulting current are in phase.

(iii) The resultant reactance of the circuit becomes zero i.e.

$$X = (X_L - X_C) = 0$$

(iv) Current in the circuit is maximum and it depends upon R.

$$I_{max} = \frac{E}{R}$$

(v) The power drawn by the circuit from the source of emf is maximum.

(vi) The potential difference V_R across the resistance R becomes equal to the applied emf.

(vii) The potential difference across the inductances is equal and opposite to the potential difference across capacitor, hence net potential difference, across the combinations of L & C is zero.

The curves plotted for I and Z against the frequency are called resonance curves. At resonant frequency the current I is maximum while impedance Z is minimum.

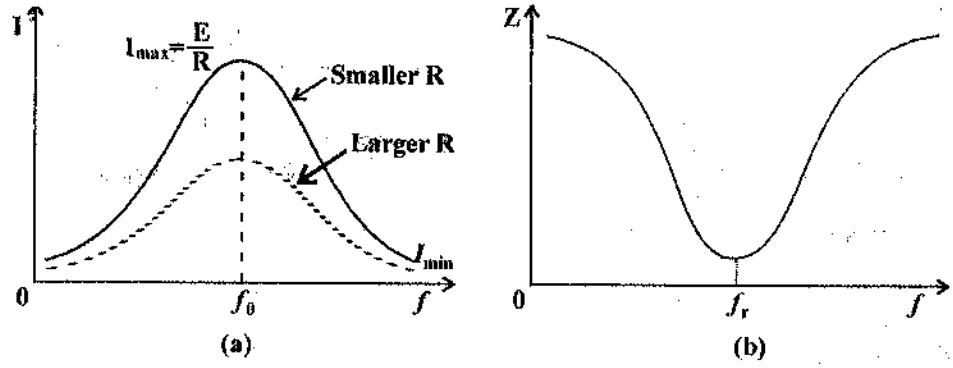


Figure: 3.24

Ex. 6 A capacitor C of 0.1 μF is used on the mains frequency of 50 Hz. Determine the reactance.

Solution: $X_C=\frac{1}{2\pi fC}$

$$X_C=\frac{1}{2\times3.14\times50\times0.1\times10^{-6}}$$

$$X_C=\frac{10^6}{2\times3.14\times50\times0.1}=3200\,\text{Ohm.}$$

Ex. 7. The capacity of a condenssor is 100 pF. Determine its reactance at 10 kHz.

Solution: $X_C=\frac{1}{\omega C}=\frac{1}{2\pi nC}$

Given value $n=10\,\text{kHz}=10\times10^3\,\text{Hz}$;

$$C=100\,\text{pF}=100\times10^{-12}\,\text{F}$$

$\therefore$ $$X_C=\frac{1}{2\pi\times10^4\times100\times10^{-12}}$$

$$X_C=\frac{10^6}{2\pi}=1.592\times10^5\,\Omega$$

Ex. 8. An inductance coil of inductance L is used in a circuit is which the frequency of AC is 50 Hz. What should be the value of L so that it may produce an impedance of 50 ohms?

Solution: $X_L=\omega L=2\pi nL$

Given value $X_L=50\,\Omega$, $n=50\,\text{Hz}$

$\therefore$ $$L=\frac{X_L}{2\pi n}=\frac{50}{2\pi\times50}=\frac{1}{2\pi}=0.159\,\text{H}$$

Ex.9. A capacitor of capacitance 79.5 μF is connected in series with a non inductive resistance of 30 Ω across 100 V. 50 Hz supply. Calculate impedance, current and maximum value of current.

Soluiton: Given value $C=79.5\,\mu\text{F}=79.5\times10^{-6}\,\text{F}$, $R=30\,\Omega$, $V=100\,\text{Volt}$, $f=50\,\text{Hz}$

As $$X_C=\frac{1}{2\pi fC}$$

$$X_C = \frac{1}{2\times 3.14\times 50\times 79.5\times 10^{-6}} = 40\,\Omega$$

Now impedance of coil is

$$Z = \sqrt{R^2 + (X_C)^2}$$

$$Z = \sqrt{(30)^2 + (40)^2} = 50\,\Omega$$

$\therefore$ Current $I = \frac{V}{Z} = \frac{100}{50} = 2$ Amp.

Thus, maximum value o current is

$$I_0 = \sqrt{2}\, I = \sqrt{2}\times 2 = 1.41\times 2 = 2.82 \text{ Amp.}$$

Ex.10 A coil takes a current of 2 ampere and power 200 watts from an AC source of 220 volts and 50 Hz. Determine the resistance and impedance of the coil.

Solution: Given value $E_{rms} = 220$ Volt, $n = 50$ Hz., $I_{rms} = 2$ Amp. and P = 200 Watt.

The impedance of the coil

$$Z = \frac{E_{rms}}{I_{rms}} = \frac{220}{2} = 110\,\Omega$$

Power dissipated $P = E_{rms}\, I_{rms} \cos\phi$

$$P = E_{rms}\, I_{rms} \left(\frac{R}{Z}\right)$$

$\therefore$ $$200 = 220\times 2\left(\frac{R}{110}\right)$$

So that $R = \frac{200}{4} = 50\,\Omega$

Ex.11. A coil of inductance 0.1 H and resistance of 10 Ω is connected to an AC source of 220 Volt (rms) and 50 Hz. Determine the impedance and reactance of the coil.

Solution: Given value $L = 0.1$H, $R = 10\,\Omega$, $n = 50$ Hz

$\therefore$ $\omega = 2\pi n = 2\pi\times 50 = 314$ rad/s.

Impedance $|Z| = (R^2 + \omega^2 L^2)^{1/2}$

$$|Z| = [100 + (314\times 0.1)^2]^{1/2}$$

$$|Z| = (100 + 985.8)^{1/2} = 32.9\,\Omega$$

Rectance of coil $X_L = \omega L$

$$= 314\times 0.1 = 31.4\,\Omega$$

Ex.12. A coil has an inductanceof 2 H. What is its reactance when $f = 50\,Hz$ and $f = 1000\,Hz$? Also calculate the susceptance in the two cases. If a current of 10 mA is passing through the coil, what is the p.d. at its ends in the two cases?

Solution: (a) $X_L = 2\pi f L = 2\times\pi\times 50\times 2$

$$= 200\pi = 628\,\Omega$$

Susceptance $= \frac{1}{X} = \frac{1}{628} = 0.001592$ mho

p.d. at its end $= I_{max} \times X_L = \left(\frac{10}{1000}\right) \times 628 = 6.28$ volts.

(b) $X_L = 2\pi f L = 2\pi \times 1000 \times 2 = 12,260\,\Omega$

Susceptance $= \frac{1}{X_L} = \frac{1}{12260} = 8.158 \times 10^{-5}$ mho

p.d. at its ends $= I_{rms} \times X_L$

$= \left(\frac{10}{1000}\right) \times 12260 = 122.6$ Volts

Ex.13. A resistance of 100 ohms and an inductance of 50 millihenries are put in series with an AC of I_{rms} = 50 Volts at 50 C/s. Calcualte the current in circuit and its phase lag, p.d. at the ends of the resistance and at the ends of the coil.

Soluiton: $Z = \sqrt{R^2 + \omega^2 L^2} = \sqrt{R^2 + (2\pi f L)^2}$

$$Z = \sqrt{(100) + (2 \times 3.14 \times 50\left(\frac{50}{1000}\right)^2} = 101.2$$

Current in the dcircuit $Z = \frac{50}{101.2} = 0.494$ Amp.

Angle of lag, $\theta = \tan^{-1} \frac{\omega L}{R} = \tan^{-1} \frac{2\pi f L}{R}$

$\theta = \tan^{-1}(0.157) = 8.55'$

p.d. at the ends of the resistance

$= I_{rms} \times R = 0.494 \times 100 = 49.4$ Volts.

p.d. atthe ends of the coil

$= 2\pi f L \times I_{rms} = 15.7 \times 0.494 = 7.76$ Volts.

p.d. of 7.76 volts is ahead of p.d. 49.4 voltas by $\pi/2$.

Ex.14. (a) Calculate the inductanceof a choke coil to be included in an AC circuit to light a 10 Watt, 20 Volt bulf on 200 Volt, 50 C/s mains.

Solution: The current through the bulb

$= \frac{\text{Power}}{\text{p.d.}} = \frac{10}{20} = 0.5$ Amp.

p.d. at the ends of the inductance (choke) $= \omega L I$

This will lead the p.d. across the resistance (bulb) by $\pi/2$, therefore

$(200)^2 = (20)^2 + (\omega L I)^2$

$\omega^2 L^2 I^2 = (200)^2 - (20)^2 = 39,600$

$\omega L I = 199$

Now $\omega = 2\pi f = 2 \times 3.14 \times 50$

and $I = 0.5$

$$\therefore \quad L = \frac{199}{0.5 \times 2 \times 3.14 \times 50} = 1.27 \text{ H.}$$

Ex.15. A capacitor $C = 1\mu F$ is used in a radio circuit where the frequency is 1000 Hz. and the current flowing is 2 mA (rms). Calculate the voltage across C. What current flows when an AC voltage of 20 Vrms, $f = 50$ Hz is connected to this capacitor?

Soluiton: **(i)** Reactance

$$X_C = \frac{1}{2\pi f C} = \frac{1}{2\pi \times 1000 \times 10^{-6}} = 159\Omega$$

$$\therefore \quad V = IX_C = \frac{2}{1000} \times 159 = 0.32 \text{ Volt}$$

(ii) When $20 V_{rms}$, $f = 50$ Hz, is connected to C, the reactance of C changes. Since $X_C = \frac{1}{f}$.

X_C at $f = 50$ Hz is 20 times X_C at $f = 1000$ Hz.

So $X_C = 20 \times 159\Omega = 3180\Omega$

$$\therefore \quad I = \frac{V}{X_C} = \frac{20}{3180} = 6.3 \times 10^{-3} \text{ Amp.}$$

Ex.16. A pure inductive coil allows a current of 10 Amp to flow from a 220 Volts, 50 Hz supply. Find, inductive reactance and inductance of coil.

Solution: Given value $i = 10$, $v = 220$ Volt and $f = 50$ Hz.

As. $i = \frac{V}{X_L}$ $\qquad X_L = \frac{V}{i} = \frac{220}{10} = 22\Omega$

Now $X_L = 2\pi f L$

$$22 = 2 \times 3.14 \times 50 \times L$$

$$L = \frac{22}{2 \times 3.14 \times 50} = 0.070 \text{ Hz}$$

3.5 Q–FACTOR, HALF POWER POINTS, BAND–WIDTH OF A SERIES RESONANT CIRCUIT

3.5.1 Q–Factor

In the case of resonance, the potential difference buildup across L or C components is much greater than the applied emf. This voltage magnification produced by resonance is called Q–factor of series resonant circuit.

Q–factor = Voltage magnification

$$= \frac{\text{Voltage developed across L or C}}{\text{Applied Voltage}}$$

$$Q = \frac{I X_L}{I R} = \frac{X_L}{R} = \frac{\omega L}{R} \qquad \text{....(29)}$$

Since we know that $f_0 = \frac{1}{2\pi\sqrt{LC}}$

$$\omega = \frac{1}{\sqrt{LC}}$$

Substituting the value of ω in Q,

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} \qquad \text{.....(30)}$$

3.5.2 Half Power Points

In a LCR series circuit

$$Z = \sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}$$

and the peak current in the circuit is

$$I_0 = \frac{E_0}{Z} = \frac{E_0}{\sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}}$$

At the condition of resonance, i.e., $\omega L = \frac{1}{\omega C}$

$$Z = Z_{min} = R$$

and $$I_{max} = \frac{E_0}{R}$$

Thus in the state of resonance, impedance will be minimum and current will be maximum.

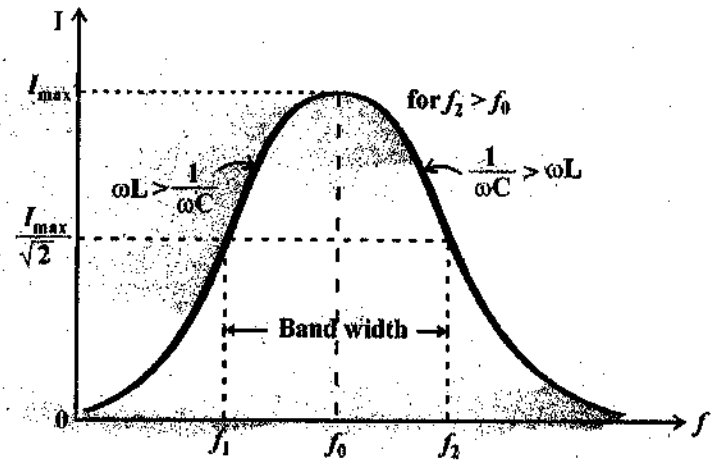


Figure: 3.25

When the frequency $f = \frac{\omega}{2\pi}$ is changed the impedance and current of circuit is shanged, when f is more than f_0, the inductive reactance (ωL) is more than compacitive reactance $\frac{1}{\omega C}$ and thus resultant impedance is more than Z_{min}. Similarly, when the frequency f is less than the resonant frequency f_0, the capacitive reactanee becomes more than inductive reactance and hence again the impedance becomes more than the minimum value (Z_{min}). Thus $f > f_0$ or $f < f_0$ the impedance increases and current decreases. The variation of current with frequency is shown in Figure (3.25). It is cleare from curve, that at $f = f_0$ the value of current is maximum and on both sides of f_0, $f > f_0$ or $f < f_0$ the current decreases. Therefore, there can be two frequancies f_1 and f_2 at

which the current in the circuit is $\frac{1}{\sqrt{2}}$ times the maximum current I_{max}. Since the power in the circuit is proportional to square of current, the power at these frequencies f_1 and f_2 are therefore called half power frequencies and the corresponding points are called half power points.

3.5.3 Band–Width

The band-width of a series resonant circuit is defined as the range of frequency over which circuit current is equal to or greater than 70.7% of maximum current.

Hence the frequency interval $(f_2 - f_1)$ is called bandwith of the cirucit.

$\therefore$ Band-width $\Delta f = f_2 - f_1$ ...(31)

Mathematically analysis gives the value of Δf equal to $\frac{1}{2\pi}\left(\frac{R}{L}\right)$.

Smaller bandwidth gives a sharper resonance and larger band width.

3.6 PARALLEL LCR CIRCUIT

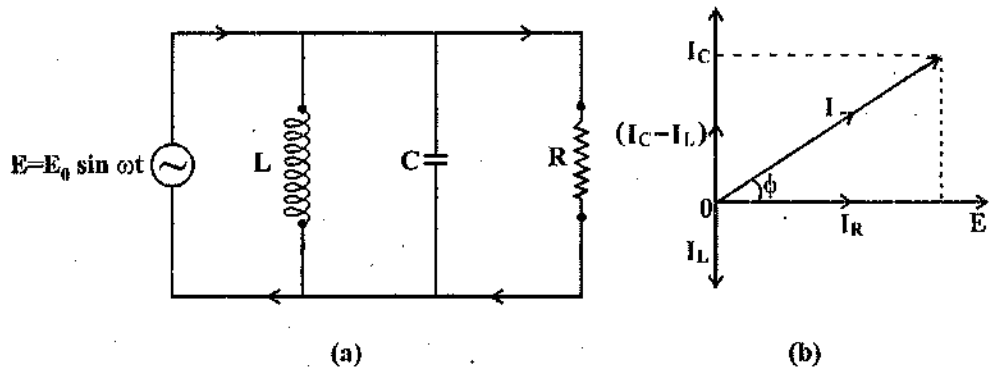


Figure: 3.26

Suppose and inductor (L) of negligible resistance, a capacitor (C) and resistance are connected in parallel in a circuit. In this circit the voltage across L, C and R are same but currents through them will be different. Total current in the circuit is the vector sum of currents in three branches. The vector diagram of current in parallel circuit is shown in Figure (3.26 b).

Thus, peak value of currents flowing-through R, L and C are:

$$I_R = \frac{E_0}{R} \quad \text{....(32)}$$

The current in R will be in phase with applied emf.

$$I_L = \frac{E_0}{X_L} = \frac{E_0}{\omega L} \quad \text{.....(33)}$$

The current lags behind the applied emf by $\pi/2$

$$I_C = \frac{E_0}{X_C} = E_0 \omega_C \quad \text{.....(34)}$$

The current lead to the applied emf. by $\pi/2$

Hence the peak value of total current will be–

$$I_0 = \sqrt{I_R^2 + (I_C - I_L)^2}$$

$$I_0 = \sqrt{\frac{E_0^2}{R^2} + \left(E_0 \omega C - \frac{E_0}{\omega L}\right)^2}$$

$$I = E_0\sqrt{\frac{1}{R^2}+\left(\omega C-\frac{1}{\omega L}\right)^2} \qquad \text{.....(35)}$$

Therefore, the impedance of the circuit will be–

$$Z=\frac{E_0}{I_0}=\frac{1}{\left[\frac{1}{R^2}+\left(\omega C-\frac{1}{\omega L}\right)^2\right]^{1/2}} \qquad \text{.....(36)}$$

From vector diagram, the phase angle between current and voltage is ϕ'

$$\tan\phi'=\frac{I_C-I_L}{I_R}=\frac{E_0\omega C-\frac{E_0}{\omega L}}{E_0R}=R\left(\omega C-\frac{1}{\omega L}\right) \qquad \text{.....(37)}$$

From equation (35) and (36) it is clear that current and impedance depends on frequency. Variation of I and Z with respect to frequency are shown in Figure (3.27a) and (3.27b).

In parallel LCR circuit, when X_L becomes equal to X_C this state is called antiresonance state. In this case resultant reactance is:

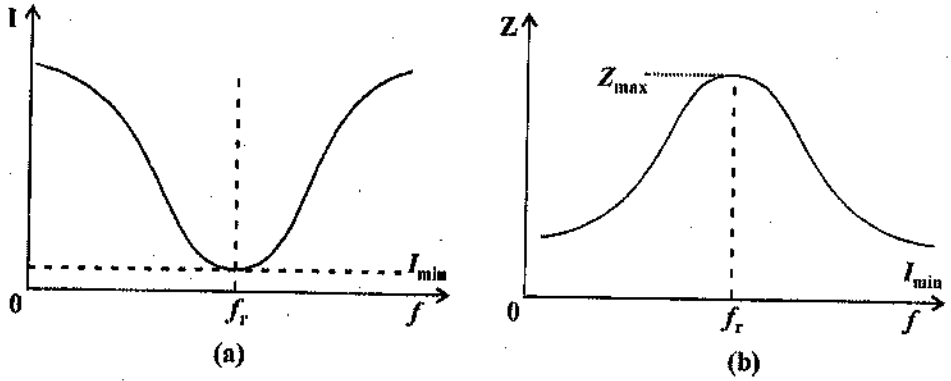


Figure: 3.27

$$X=\frac{X_LX_C}{X_L-X_C} \qquad \text{....(38)}$$

So at resonance, i.e., $\omega L=\frac{1}{\omega C}$

$X=\infty$ (infinity)

Thus in the state of resonance, the impedance of the cirucit will be maximum and the current flowing through it will be minimum.

3.7 POWER IN AC CIRCUIT

The energy dissipated per second (work done by the current per second) is called power. It is equal to the product of voltage and current. The power in AC circuit depends on the phase difference between voltage and current.

Let at any time t, alternating current and emf are expressed as

$$E=E_0\sin\omega t$$

$$I=I_0\sin(\omega t-\phi)$$

where ϕ is the phase difference between E and I.

Therefore, instantaneous power in AC circuit will be

$$P = E\,I \qquad \text{.....(39)}$$

$$= E_0 I_0 \sin\omega t \sin(\omega t - \phi)$$

using trignometric relation

$$\sin C \sin D = \frac{1}{2}[\cos(C - D) - \cos(C + D)]$$

we get $$P = \frac{1}{2} E_0 I_0 \{\cos[\omega t - (\omega t - \phi)] - \cos(\omega t + \omega t - \phi)\}$$

$$= \frac{1}{2} E_0 I_0 \{\cos\phi - \cos(2\omega t - \phi)\}$$

$$= \frac{1}{2} E_0 I_0 \cos\phi - \frac{1}{2} E_0 I_0 \cos(2\omega t - \phi) \qquad \text{....(40)}$$

Equation (40) has two terms: (i) $= \frac{1}{2} E_0 I_0 \cos\phi$ does not depends on time and (ii) $\frac{1}{2} E_0 I_0 \cos(2\omega t - \phi)$ varies periodically with time.

For a complete cycle, the average value of the $\cos(2\omega t - \phi)$ is zero.

Hence average power for one complete cycle is

$$P_{av} = \frac{1}{2} E_0 I_0 \cos\phi$$

$$P_{av} = \left(\frac{E_0}{\sqrt{2}}\right)\left(\frac{I_0}{\sqrt{2}}\right)\cos\phi \qquad \text{....(41)}$$

$$P_{av} = E_{rms}\, I_{rms} \cos\phi \qquad \text{.....(42)}$$

The factor $\cos\phi$ present in the expression is called power factor.

(i) Circuit containing resistance only

$\therefore$ Phase angle $\phi = 0$

Power factor $\cos\phi = 1$

$\therefore$ $P_{av} = \frac{1}{2} E_0\, I_0 = E_{rms}\, I_{rms}$

(ii) Circuit containing pure inductance only

Q Voltrage leads the current by $\pi/2$ i.e. $\phi = \pi/2$

Power factor $\cos\phi = 0$

$\therefore$ $P_{av} = 0$

(iii) Circuit containing pure capacitance only–

Q Voltage lags behind the current by $\pi/2$, i.e. $\phi = -\pi/2$

Power factor $\cos\phi = 0$

Q $P_{av} = 0$

(iv) For a series LCR circuit:–

Q $$\tan\phi = \frac{\omega L - \frac{1}{\omega C}}{R} = \frac{X}{R}$$

$\therefore$ $$\cos\phi = \frac{R}{\sqrt{R^2 + X^2}}$$

$$\cos\phi = \frac{R}{\sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}}$$

At resonance condition voltage and current are in same phase; i.e. $\phi = 0$

Power factor $\cos\phi = 1$

$$P_{av} = \frac{1}{2} E_0 I_0 = E_{rms} I_{rms}$$

Ex.17 In a series L–C–R circuit L = 1 mH, C = 10 μF and R = 10Ω. Determien the resonant frequency. What will be the band-width when (i) R = 1Ω and (ii) R = 0.1Ω?

Solution: Given value $L = 10^{-3}$ H, $C = 10 \times 10^{-6}$ F, $R = 10\Omega$.

The resonant frequency is given by

$$\omega_0 = \frac{1}{\sqrt{LC}} = \frac{1}{(10^{-3} \times 10^{-3})^{1/2}} = 10^4$$

$$\therefore \quad f_0 = \frac{10^4}{2\pi} = 1592 \text{ Hz}$$

(i) Band-width at $R = 1\Omega$

$$\Delta f = (f_2 - f_1) = \frac{1}{2\pi} \frac{R}{L}$$

$$\Delta f = \frac{1}{2\pi \times 10^{-3}} = \frac{1000}{2\pi} = 159.2 \text{ Hz}$$

Ex.18 A coil of inductance 0.4 H and negligible resistance is connected in series with a resistance of 120 Ω. Generatign voltage of 100 V (rms) and frequency $(200/\pi)$ Hz is applied on the combination. Calculate (i) Impedance of the circuit, (ii) Power factor (iii) Phase difference between E and I and (iv) Average power.

Solution: Given value $L = 0.4$ H, $R = 120\Omega$,

$$n = \frac{200}{\pi} \text{ Hz and } E_{rms} = 100 \text{ V}.$$

$$\therefore \quad \omega = 2\pi n = 2\pi \times \frac{200}{\pi} = 400 \text{ rad/s}$$

Reactance of the coil $X_L = \omega L = 400 \times 0.4 = 160\Omega$

(i) Impedance of the circuit

$$Z = (R^2 + \omega^2 L^2)^{1/2}$$

$$Z = (120^2 + 160^2)^{1/2}$$

$$Z = 10(144 + 256)^{1/2} = 200\Omega$$

(ii) Power factor $\cos\phi = \frac{R}{Z} = \frac{120}{200} = 0.6$

(iii) Phase difference between voltage and current

$$\phi = \tan^{-1}\left(\frac{\omega L}{R}\right) = \tan^{-1}\left(\frac{160}{120}\right)$$

$$\phi = \tan^{-1}\left(\frac{4}{3}\right)$$

(iv) Current in the circuit

$$I_{rms} = \frac{E_{rms}}{Z} = \frac{100}{200} = 0.5 \text{ Amp.}$$

$\therefore$ Average power $\bar{P} = E_{rms}\, I_{rms} \cos\phi$

$$\bar{P} = 100 \times 0.5 \times 0.6 = 30 \text{ Watt}$$

Ex.19 An iron-cored coil of 2H and 50 Ω resistance is placed in series with a resistor of 450 Ω na 100 V, 50 Hz, AC supply is connected across the arrangement. Calculate

(a) the current flowing in the coil.

(b) itsphase angle relative to the voltage supply.

(c) the voltageacross the coil.

Solution: (a) The reactance

$$X_L = 2\pi f L = 2\pi 50 \times 2 = 628\,\Omega$$

$\therefore$ Circuit impedance

$$Z = \sqrt{X_L^2 + R^2} = \sqrt{628^2 + 500^2} = 803\,\Omega$$

$\therefore$ $$I = \frac{V}{Z} = \frac{100}{803} \text{ Amp.} = 12.5 \text{ mili Amp.}$$

(b) $\tan\theta = \frac{X_L}{r} = \frac{628}{500} = 1.256$

So $\theta = 51.5°$

(c) For the coil $X_L = 628\,\Omega$ and $R = 50\,\Omega$

So coil impedance $Z = \sqrt{X_L^2 + R^2} = \sqrt{628^2 + 50^2} = 630\,\Omega$

$\therefore$ Voltage across coil $V = I \times Z = 12.5 \times 10^{-3} \times 630 = 7.9$ Volt.

3.8 SUMMARY

- Rate flow of charge is called current.
- Current which flows continuously in a definite direction with constant magnitude is called Direct Current (D.C.)
- An alternating current is an electric current which changes it magnitude and direction after a regular time of interval with respect to time. It is of two types, sinusoidal and non-sinusoidal.
- At a particular instant, the value of voltage or current is called instantaneous value.
- In a complete cycle, the maximum value attained by alternating current or vltage is called peak value.
- The average of alternating voltage or current at a given time over a full cycle is called mean or average value.
- The square root of the mean square value is called root mean squre value.
- Reactance and resistance of various circuits:

Resistance $= R\angle 0$ for circuit containing R only.

Inductive reactance $X_L = \omega L \angle +\pi/2$ for circuit containing L only.

Capacitive reactance $X_C = \frac{1}{\omega L} \angle -\pi/2$, for circuit containing C only.

Where the angle given with resistance, reactance is the phase difference between voltage and current.

- Impedance (reactance) of complex circuitis containing more than one elements is series:

For R–L circuit $Z_{RL} = \left(R^2 + \omega^2 L^2\right)^{1/2}$

For R–C circuit $Z_{RC} = \left(R^2 + \frac{1}{\omega^2 C^2}\right)^{1/2}$

For LCR circuit $Z_{LRC} = \left(R^2 + (X_L - X_C)^2\right)^{1/2}$

For LC circuit $Z_{LC} = \left(\omega L^2 - \frac{1}{\omega C}\right)$

- In parallel LCR circuit

Impedance $Z'_{LCR} = \frac{1}{\left[\frac{1}{R^2} + \left(\omega L - \frac{1}{\omega L}\right)^2\right]^{1/2}}$

and phase angle $\tan\phi' = \left(\omega C - \frac{1}{\omega C}\right)R$

- In LCR series circuit, when $X_L \approx X_C$ i.e. $\omega L = \frac{1}{\omega C}$, the impedance of the circuit will be minimum (equal to resistance only). Therefore, at frequency $\omega = \frac{1}{\sqrt{LC}}$ current will be maximum. This state is called electrical resomance of the circuit.

- In parallel LCR circuit, when $X_L = X_C$, this stateis called anti resonant state. In this state impedanceis maximum and current is minimum.

- The frequencies at which the power in the circuit is half of the power at resonant frequency are called half power points.

- Power of an AC circuit depends upon the phase difference between voltage and current.

$$P_{av} = E_{rms} I_{rms} \cos\phi$$

- The term $\cos\phi$ is known as power factor.

3.9 REVIEW QUESTIONS

Q.1. Explain the difference between ohmic and non-ohmic resistances by giving one example for each.

Q.2. Why are copper wires used as connecting wire in a circuit.

Q.3. How does the resistance of filament of a bulb depend on its power rating?

Q.4. What is time constant for R–C circuit?

Q.5. What is meant by alternating current? Write it's type.

Q.6. What is inductive reactance?

Q.7. Explain phase & phase difference.

Q.8. An inductor, a capacitor and a resistor are connected in a series to an AC source. Write expression for impedance Z and phase angle ϕ.

Q.9. What is power factor for L–C–R, A.C. circuit. What are its maximum & minimum values and under what condition.

Q.10. Define Q-factor and band width for series resonant Circuit.

Q.11. What is necessary condition for series and parallel resonating circuits. Write down the expression for frequency in each resonanting position.

Q.12. In an alternating current circuit, an inductance L, a capacitance C and a resistance R are connected in series. Derive expression for impedance and phase angle.

Q.13. Draw series resonant circuit for L–C–R combination. Write the formula for impedance & resonant frequency of this ciruit.

Q.14. What is an alteranting current?

Q.15. Establish an expression for emf induced in a coil when it is roated about an axis in a uniform magnetic field with angular velocity ω.

Q.16. The equation of an AC source is given by $I = 4\sin(100\pi t - \theta)$. Find out time period for current.

Q.17. An alteranting voltage is given by $I = 14.1\sin(6280t + \pi/3)$. Find rms value of current and it's frequency.

Q.18. In L–C–R circuit, a voltmeter reads 80 V across resistance, 100 V across inductance and 40 V across capacitor. Calculate, value of electromotive force applied to circuit.

Q.19. The power factor of an A.C. circuit is 0.5. Calculate impedance of circuit if resistance of circuit is 10Ω.

Q.20. Calcute capacitive reactance of a capacitor of capacitance $60\mu F$ at frequency of 600 Hz.

◉◉◉◉

Unit-04
ELECTRICAL WIRING

Content of the Unit

4.0 OBJECTIVE

In this chapter we will discuss –

- An electric power system consists of major parts such as generators, transformers etc.
- To provide safety to these major parts of the system from lightening strokes and earth faults it is necessary to provide earthing.
- A network of wiring connecting various accessories for distribution of electrical energy from the supplier meter board to the numerous electrical energy consuming devices is known as a wiring system.
- In this chapter we shall study the important applications of the phenomenon of electromagnetic induction like D.C. generator, D.C. motor and transformer etc.

4.1 INTRODUCTION

It is well known that whenever an electric current flows through a conductor, a magnetic field is imme-

diately exist in the space surrounding the conductor. We can say that when electrons are in motion they produce a magnetic field. The converse of this is also true i.e. when a magnetic field embracing a conduct or moves relative to the conductor, it produces a flow of electrons. This phenomenon whereby an emf and hence current is induced in any conductor is known as electromagnetic induction. Now by using the principle of production of induced e.m.f. various machines such as generators, transformers and motors are used to convert mechanical energy into electrical energy.

A network of wires connecting various accessories for distribution of electrical energy from the supplier meter board to the numerous electrical energy consuming devices and other domestic appliances through controlling and safety devices is known as a wiring system. In an electrical installation, if a metallic part of an electric appliance comes in direct contact with a bare or live wire the metal being a good conductor of electricity is charged and static charge on it will accumulate. But if the metallic part of the appliances are earthed, the charge will be transferred to the earth immediately. Thus earthing of metallic parts of electrical equipment and appliances provides safety.

4.2 THREE PHASE AC CIRCUIT

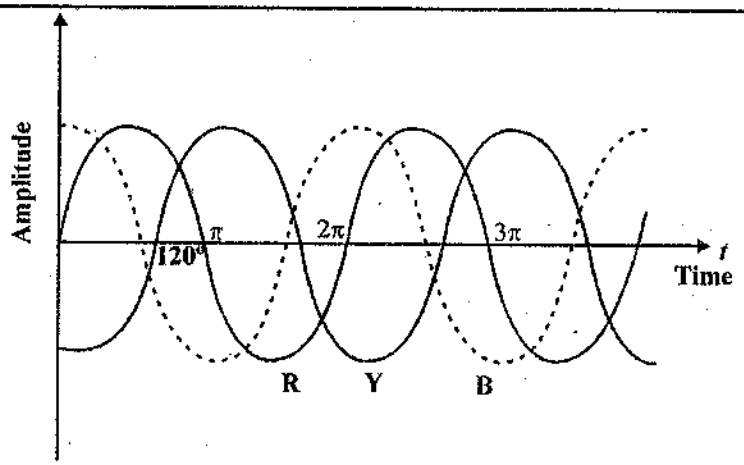


Figure 4.1: Represents the Graphical Pattern of Voltages in Three Phase Circuit.

Electrical circuit which are excited by three phase energy sources are called three phase AC circuits. A three phase circuit has three terminals (phase) which are called lines. It may or may not have a fourth terminal called neutral. The neutral is a reference terminal. In three phase circuit each terminal (phase) has it's own voltage. So there are three voltages in three phase circuit and consequently three currents in the three conductors, that constitute three-phase system. The currents will be usually lagging behind the voltages by their respective phase angles. In unbalanced circuit resultant current will flow in the neutral wire. A three phase ac circuit may be treated as three separate single phase system and phase displaced from each other by 120^0 or $\frac{2\pi}{3}$ radians and peaks of the respective voltages do not occur simultaneously.

Three phase ac system is universally adopted system for generation, transmission and distribution of electrical power.

4.3 GENERATION OF THREE PHASE VOLTAGES SYSTEM

An ac system having a group of three voltages of some frequency arranged to have equal phase difference between adjacent e.m.f.'s called a (3-ϕ) three phase system. Consider three identical coils A(a, a'), B(b, b') and C(c, c') mounted as shown in Figure (4.2 a and b). Here a, b and c are the start terminals of the three coils. A phase difference of 120^0 electrically is maintained between the corresponding start terminals a, b and c. Let the three coils mounted on same axis be rotated with in a stationary magnetic field or the magnetic field system be rotated keeping coils stationary in anti clockwise direction at an angular speed of ϕ radian/ sec as shown in Figure (4.2 a and b) respectively.

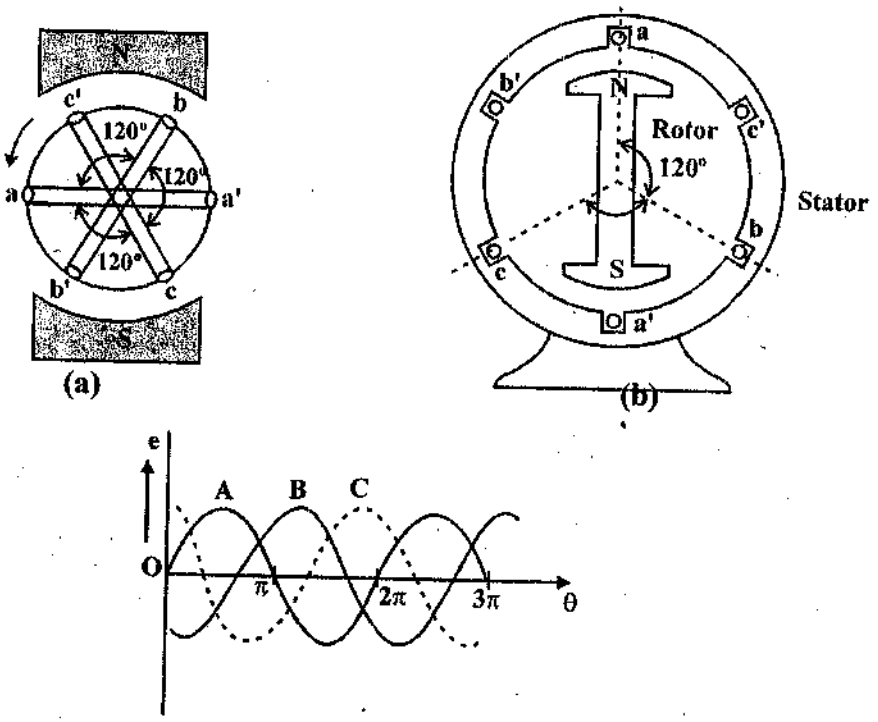


Figure 4.2: Magnitude and Direction of e.m.f.'s.

Three e.m.f's $e_{aa'}$, $e_{bb'}$ and $e_{cc'}$ are induced in the three coils. The magnitude and direction of these emf's at this instant, are given

(a) The induced e.m.f. $e_{aa'}$ in coil aa' is zero and increasing in the positive direction as shown by wave form of $e_{aa'}$ in Figure (4.2 c).

Equation of this e.m.f. can be represented by $e_{a,a'} = E_m \sin \omega t$

(b) The coil b, b' is 120° (electrical) behind the coil a, a'. The induced emf in this coil is negative and is become maximum negative as shown by waveform $e_{b,b'}$ in Figure (4.2 c). The equation of this emf can be represented by $e_{b,b'} = E_m Sin(\omega t - 120^0)$.

(c) The coil c, c' is 120° (electrical) behind coil b, b' or 240° (electrical) behind coil a, a'. The induced emf in the coil is positive and is decreasing as shown by waveform $e_{c,c'}$ in Figure (4.2 c). The equation of this is represented by $e_{c,c'} = E_m Sin(\omega t - 240^0)$.

Advantages of 3–Phase System over a Single Phase System

(a) Three phase generators are more economical and efficient.
(b) For a given size of frame the output of a 3-phase ac system is greater than that of a single phase system.
(c) Transmission of electrical power using three phase ac system is cheaper than single phase ac system.
(d) For the same output and same speed the power factor of 3-phase motor is very good as compare to a single phase motor.
(e) Voltage regulation of 3-phase system is better.

4.4 DC GENERATOR

It is a device which is used for producing direct current energy from mechanical energy.

4.4.1 Principle

The principle of dc generator is based on the phenomenon of electromagnetic induction i.e. whenever amount of magnetic flux linked with a coil changes, an emf is induced in the coil. It lasts so long as the

change in magnetic flux through the coil continues.

4.4.2 Construction

The essential parts of a dc generator are shown in Figure (4.3 a).

(1) Armature

ABCD is a rectangular armature coil. It consists of a large number of turns of insulated copper wire wound over a laminated soft iron core I. The coil can be rotated about the central axis.

(2) Field Magnets

N and S are the pole pieces of strong electromagnet in which the armature coil is rotated. Axis of rotation is perpendicular to the magnetic field lines.

(3) Split Rings

R_1 and R_2 are two halves of the rings to which two ends of armature coil are connected. These rings rotate with the rotation of the coil.

(4) Brushes

B_1 and B_2 are two flexible metal plates or carbon rods. They are fixed and are kept in light contact with R_1 and R_2 respectively. The purpose of brushes is to pass an current from the armature coil to the external load resistance R.

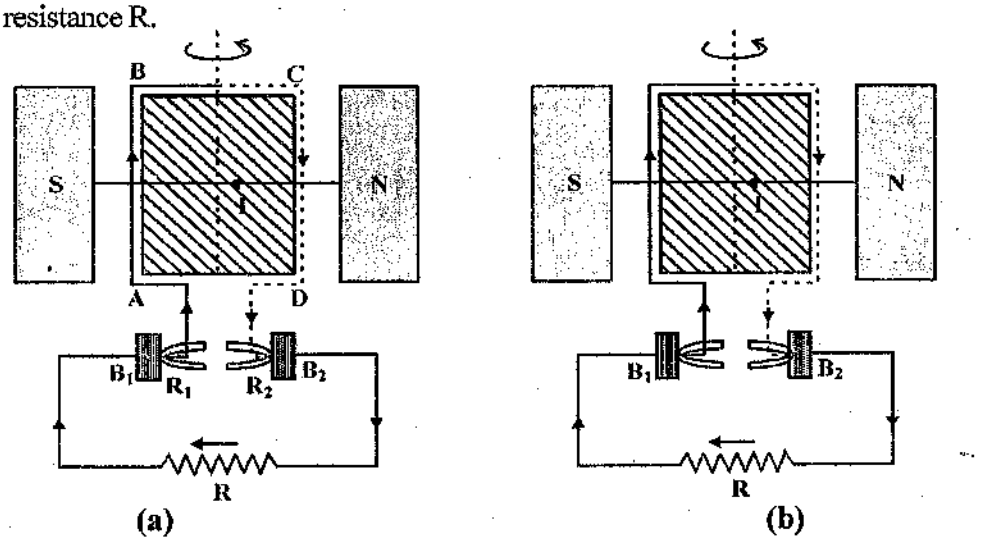


Figure 4.3: D.C. Generator.

4.4.3 Working

To start with we assume that the plane of the coil is perpendicular to the plane of the paper in which magnetic field is applied.

Let us suppose that the armature coil ABCD is moving in such a way that the arm AB moves inwards and CD moves outwards. Then applying Fleming's right hand rule, we see that the current flows in the armature as shown in Figure (4.3 a).

After the armature coil has rotated through 180, it occupies the position as shown in Figure (4.3 b). Now CD is moving inwards and AB is moving outwards. Then again applying Fleming's right hand rule, we find that current flows in the armature as shown in Figure (4.3 b).

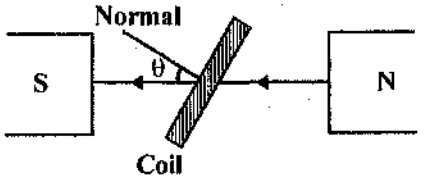


Figure: 4.4

Thus we observe that the direction of the induced e.m.f. and the induced current does not change in the external circuit during one complete rotation of the armature coil i.e. the induced current in the external circuit always flows in the same direction.

As the armature coil is rotated in the magnetic field, angle θ between the field and normal to the coil

changes continuously. Therefore magnetic flux linked with the coil changes. An e.m.f. is induced in the coil.

Magnetic flux linked with the coil according to Figure (4.4).

$$\phi = N(\vec{B}.\vec{A}) = NBACos\theta = NBA\,Cos\omega t$$

N = number of turns in the coil

B = strength of magnetic field

A = area enclosed by each turn of the coil

θ = angle which normal to the coil makes with B at any instant t

ω is the angular velocity of the coil.

If 'e' is the e.m.f. induced in the coil, then

$$e = -\frac{d\phi}{dt} \equiv -\frac{d}{dt}(NBA\cos\omega t)$$

$$= -NBA\frac{d}{dt}(\cos\omega t)$$

$$= -NBA(-\sin\omega t).\omega$$

$$= NBA\,\omega\sin\omega t$$

The induced e.m.f. will be maximum, when $\sin\omega t$ = maximum = 1

$$e_{max} = e_0 = NBA\omega \times 1 = NBA\omega$$

$$e = e_0 Sin\,\omega t$$

The variation of 'e' with time in dc generator is as shown in Figure (4.5).

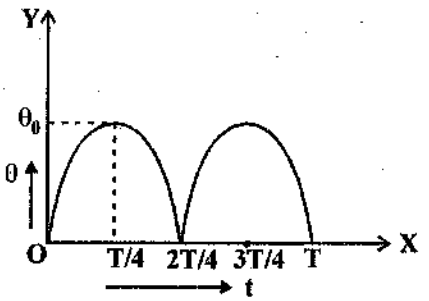


Figure 4.5: Variation of e with time in DC generator.

The direction of 'e' is not reversed in the second half cycle as explained in the working. It happens because after half the rotation of the coil R_1 goes in contact with B_2 and R_2 goes in contact with B_1.

The current produced in a simple dc generator is shown in Figure (4.5). This current is unidirectional but its value varies considerably and falls even to zero value twice during each rotation of the coil. When we use a number of coils equally inclined to one another, with the commutator ring divided into as many segments as the total number of ends of the coils, then each coil works independently sending it's own current into the outer circuit. The resultant current/ e.m.f. so obtained is shown in Figure (4.6). The value is almost constant in magnitude and direction of course is the same.

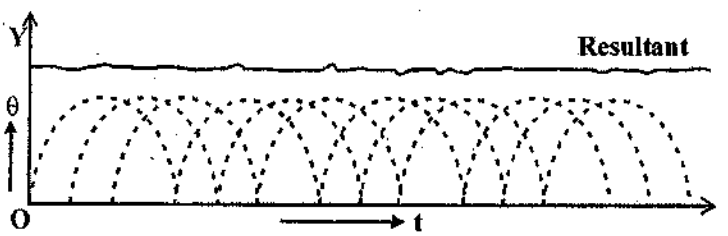


Figure 4.6: Resultant Current / emf.

4.5 D.C.MOTOR

A DC motor converts direct current energy from a battery into mechanical eergy of rotation.

4.5.1 Principle

It is based on the fact that when a coil carrying current is held in a magnetic field, it experiences a torque, which rotates the coil.

4.5.2 Construction

It consists of the following five parts:

(1) Armature Coil

The armature coil ABCD consists of a large number of turns of insulated copper wire wound over a soft iron core.

(2) Field Magnet

The magnetic field is supplied by a permanent magnet NS.

(3) Split Rings or Commutator

These are two halves of the same ring. The end of the armature coil is connected to these halves which also rotate with the armature.

(4) Brushes

These are two flexible metal plates or carbon rods B_1 and B_2, which are so fixed that they constantly touch the revolving rings.

(5) Battery

The battery consists of a few cells of voltage V connected across the brushes. The brushes convey the current to the rings from where it is carried to the armature.

4.5.3 Working

The battery sends current through the armature coil in the direction shown in Figure (4.7 a). Applying Fleming's left hand rule, CD experiences a force directed inwards and perpendicular to the plane of the coil. Similarly AB experience a force directed outwards and perpendicular to the plane of the coil. These two forces being equal, unlike and parallel form a couple. The couple rotates the armature coil in the anticlockwise direction, after the coil has rotated through 180°. The direction of the current in AB and CD is reversed Figure (4.7 b). Now CD experiences an inward force. The armature coil thus continues rotating in the same i.e. anticlockwise direction.

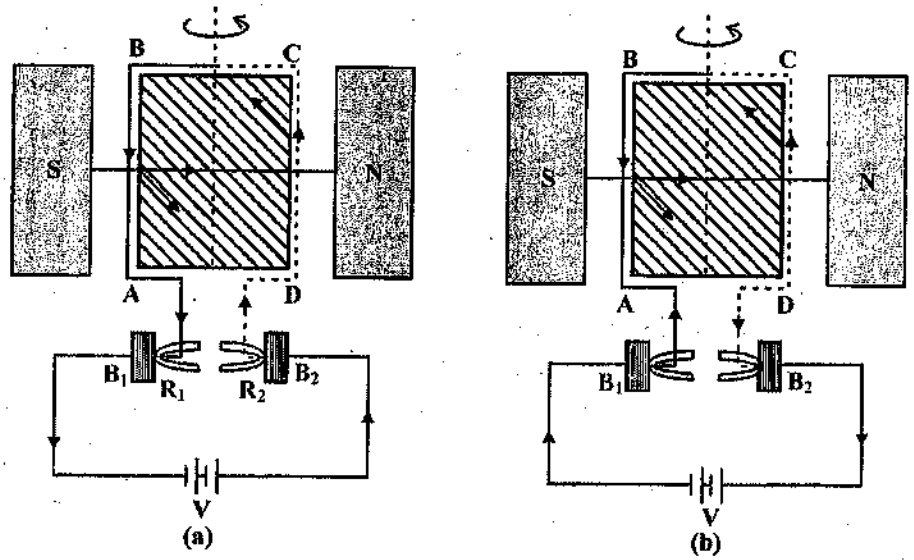


Figure 4.7: Working of D.C. Motor

As the armature rotates in the magnetic field, the amount of magnetic flux linked with the coil changes. Therefore, an e.m.f. is induced in the coil. The direction of the induced e.m.f. is such that it opposes the battery current in the circuit. This e.m.f. is known as back e.m.f. and its magnitude goes on increasing with the speed of the armature.

Let V = e.m.f. applied across B_1 and B_2
R = resistance of the armature coil
I = current flowing through the armature coil at any instant t
E = back e.m.f. at that instant
As V and E are in the opposite directions
Effective e.m.f. across B_1 and B_2 = V – E
According to ohm's law

$$I = \frac{V - E}{R}$$

$$V - E = IR$$

$$V - IR = E$$

Since the current I is being supplied to the armature coil by the external source of e.m.f. V, therefore
Input electric power = VI
Power lost in the form of heat in the coil = I^2R
Output mechanical power = $VI - I^2R = (V - IR)I = EI$

Efficiency of dc motor i.e. $\eta = \frac{\text{Output Mechanical Power}}{\text{Input Electric Power}}$

$$\eta = \frac{EI}{VI} = \frac{E}{V} = \frac{\text{back emf}}{\text{applied emf}}$$

Uses of DC Motor

(1) The dc motors are used in dc fans (exhaust, ceiling or table) for cooling and ventilation.
(2) They are used for pumping water.
(3) Big dc motors are used for running tram cars and even trains.

4.6 TRANSFORMER

A transformer is an electric device which is used to changing the AC voltages.
A transformer which increases the ac voltages is called a step up transformer. A transformer which decreases the ac voltages is called a step down transformer.

4.6.1 Principal

A transformer is based on the principle of mutual induction i.e. whenever the amount of magnsetic flux linked with a coil changes an e.m.f. is induced in the neighboring coil.

4.6.2 Construction

A transformer consists of a rectangular soft iron core made of laminated sheets, well insulated from one another. Two coils P_1, P_2 and S_1, S_2 are wound on the same core but are well insulated from each other. The source of alternating e.m.f. is connected to P_1P_2, the primary coil and a load resistance R is connected to S_1S_2, the secondary coil. Output is taken across the load resistance R, Figure (4.8)

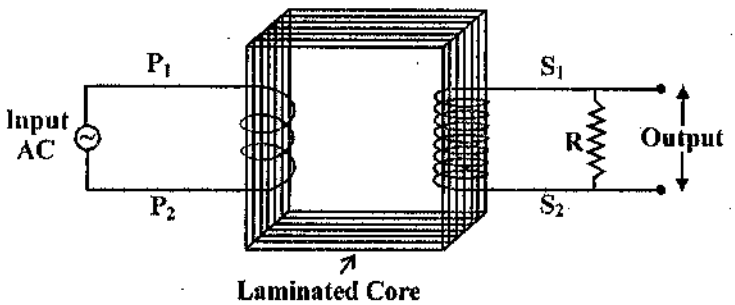


Figure 4.8: Transformer.

In step up transformer, the primary coil consists of only a few turns of thick insulated copper wire,

whereas secondary coil consists of a very large number of turns of fine insulated copper wire.
In a step down transformer, the coil S_1S_2 is make of a few turns of thick insulated copper wire, whereas coil P_1P_2 consists of a very large number of turns of fine insulated copper wire.

4.6.3 Theory and Working

As current in primary varies, the magnetic flux linked with P_1P_2 and hence with secondary S_1S_2 changes. Due to self induction, an e.m.f. is induced in P_1P_2 and due to mutual induction an e.m.f. is indused in S_1S_2.

Suppose n_p = number of turns in P_1P_2

E_p = alternating e.m.f. fed to P_1P_2 at instant t

$\frac{d\phi}{dt}$ = rate of change of magnetic flux linked with each turns of P_1P_2

under ideal conditions,

the self induced e.m.f. in P_1P_2 at instant t = e.m.f. fed to P_1P_2 at this instant

i.e. $$-n_p\frac{d\phi}{dt} = E_p$$

or $$E_p = -n_p\frac{d\phi}{dt}$$

If we assume that there is no leakage of magnetic flux, then the rate of change of magnetic flux through each turn of S_1S_2 is $= \frac{d\phi}{dt}$

If n_s is number of turns in S_1S_2, then e.m.f. induced in secondary coil due to mutual induction is

$$E_s = -n_s\frac{d\phi}{dt}$$

$$\frac{E_s}{E_p} = \frac{n_s}{n_p} = K$$

Where K is a constant called transformation ratio. It represents ratio of number of turns in the secondary to the number of turns in the primary coil of the transformer.

For a step up transformer, $E_s > E_p$, $K>1$ hence $n_s > n_p$

In a step down transformer, $E_s < E_p$, $K<1$ hence $n_s < n_p$

If I_p is the value of primary current at the same instant t and I_s is the value of secondary current at this instant, then input power at the instant $t = E_pI_p$

Output power at the same instant $= E_sI_s$

If we assume that there is no loss of power

Then output power = input power

$$E_sI_s = E_pI_p$$

$$\frac{E_s}{E_p} = \frac{I_p}{I_s} = K$$

Now efficiency of a transformer is defined as the ratio of output power t the input power

$$\eta = \frac{\text{Output power}}{\text{input power}} = \frac{E_sI_s}{E_pI_p}$$

Uses of Transformer

A transformer is used in almost all a.c. operations i.e.

(1) In voltage regulators for T.V., refrigerator, computer, air conditioner etc.
(2) In the induction furnaces
(3) For welding purposes

4.7 THREE PHASE INDUCTION MOTOR

Off all the ac motors the 3-phase induction motor is the one which is extensively used for various kinds of industrial drives. It has the following main advantages as well as disadvantages.

Advantages

(1) It has very simple and extremely rugged almost unbreakable construct

(2) Its cost is low and is very reliable.

(3) It has sufficiently high efficiency. It has a reasonable good power factor.

(4) It requires minimum maintenance.

(5) It starts up from rest and need no extra starting motor and has not to be synchronized. Its starting arrangement is simple.

Disadvantages

(1) Its speed can't be varied without sacrificing some of its efficiency.

(2) Just like dc shunt motor, its speed decreases somewhat with increase in load.

(3) Its starting toque is somewhat inferior to that of a dc shunt motor.

4.7.1 Construction

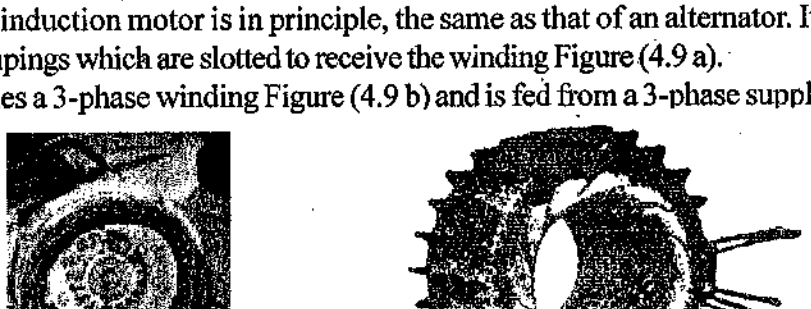
An induction motor consists of two main parts:

(i) A stator (ii) A rotor

(i) A Stator

The stator of a induction motor is in principle, the same as that of an alternator. It is made up of a number of stampings which are slotted to receive the winding Figure (4.9 a).

The stator carries a 3-phase winding Figure (4.9 b) and is fed from a 3-phase supply.



(a) (b)

Figure 4.9: (a) Unwound Stator (b) Wound Stator for an Induction Motor.

It is wound for a definite number of poles, the exact number of poles being determined by the requirements of speed. greater the number of poles,lesser the speed and vice versa. The stator windings produce a magnetic field or flux, when 3-phase current supplied, which is of constant value but which revolves or rotates at synchronous speed. This revolving magnetic flux induced an e.m.f. in the rotor by mutual induction.

(ii) Rotor

(a) Squirrel cage rotor– Motors employing this type of rotor are known as squirrel-cage induction motors.

(b) Phase-wound or wound rotor– Motors employing this type of rotor are variously known as "phase wound" motor or "wound" motors or as "slip-ring" motors.

(a) Squirrel-cage rotor:– Most of the induction motors are squirrel-cage type. The rotor consists of a cylindrical laminated core with parallel slots for carrying the rotor conductors which are not wires but consists of heavy bars of copper, aluminum or alloys. One bar is placed in each slot, rather the bars are inserted from the end when semi closed slots are used. The rotor bars are brazed or electrically welded to two heavy and slot short circuiting end-rings. This giving, a squirrel-cage construction.

(b) Phase wound rotor:– This type of rotor is provided with 3-phase, double layer, distrib-

uted winding consisting of coils as used in alternates. The rotor is wound for as many poles as number of stator poles and is always wound 3-phase even when the stator is wound two phase.

4.7.2 Principle of Operation

When the 3-phase stator windings are fed by a 3-phase supply then a magnetic flux of constant magnitude but rotating at 'Synchronous speed' is set up.

The flux passes through the air gap, sweeps past the rotor surface and so cuts the rotor conductors which are stationary. Due to the relative speed between the rotating flux and stationary conductors an e.m.f. is induced in the latter according to Faraday's law of electromagnetic induction. The frequency of the induced e.m.f. is the same as the supply frequency. Its magnitude is proportional to the relative velocity between the flux and the conductors and its direction is as given by Fleming's right hand rule. Since the rotor bars or conductors form a closed circuit, rotor current is produced whose direction is such as to oppose the very cause producing it. In this case, the cause which produce the rotor current is the relative velocity between the rotating flux of the stator and the stationary rotor conductors. Hence to reduce the relative speed, the rotor starts running in the same direction as tat of the flux and tries to catch up with the rotating flux.

4.7.3 Frequency of Rotor Current

When the motor is stationary, the frequency of rotor current is the same as the supply frequency. But when the rotor starts revolving, then the frequency depend upon the relative speed or on the slip speed. Let at any slip speed the frequency of the rotor current be f' then

$$N_s - N = \frac{120 f'}{P}$$

$$N_s = \frac{120 f}{P}$$

During one by the other, we get

$$\frac{f'}{f} = \frac{N_s - N}{N_s} = S$$

$$f' = Sf$$

4.8 SINGLE PHASE INDUCTION MOTOR

Like 3- phase motor, a single phase motor also consists of:

(i) a stator which carries single phase winding and

(ii) a squirrel-cage type of rotor

However, there is one fundamental difference between the two is a 3-phase motor is self starting, a single phase motor is non self starting. This is due to fact that the stator winding of a 3-phase motor produces a rotating (or revolving) flux, the single phase winding produces merely a pulsating or alternating flux. A synchronously rotating flux can be produced only by either a 2-phase or 3-phase stator winding when energized from a 2-phase or 3-phase supply respectively.

An alternating flux acting on a stationary squirrel-cage rotor cannot produce rotation (only a rotating flux can).

However, if the rotor of a single phase motor is given an initial start by hand or otherwise in either direction, then immediately a torque arises and motor accelerates to its final speed provided it is not heavily loaded.

4.9 MEASURING INSTRUMENTS

An instrument is defined as a device to determined the value or magnitude of a variable quantity. For measuring various electrical quantities different types of measuring instruments are used

(i) Galvanometer

(ii) Ammeter or Ampere-meter

(iii) Voltmeter and Electrometer

(iv) Wattmeter
(v) Energy meter
(vi) Frequency meter
(vii) Oscilloscopes
(viii) Multimeter etc.

The measuring instruments can be divided into two categories analog and digital. An analog instrument is a device where the output is a continuous function of it's input.

An analog instrument is one which magnitude of the measured electrical quantity is indicated by the movement of a pointer across the face of a scale The indication on a digital instrument is in the form of a series of numbers displayed on a screen. Both types of instrument have their advantages and limitations.

4.10 MULTIMETER

Multimeters are very useful test instruments. By operating a multi-position switch on the meter they can be quickly and easily set to be a voltmeter, an ammeter or an ohmmeter. They have several settings (called 'ranges') for each type of meter and the choice of AC or DC. Some multimeters have additional features such as transistor testing and ranges for measuring capacitance and frequency. The Figure (4.10) show multimeters which are suitable for general electronics use. A digital multimeter is the best choice for first multimeter, which is suitable for testing simple projects.

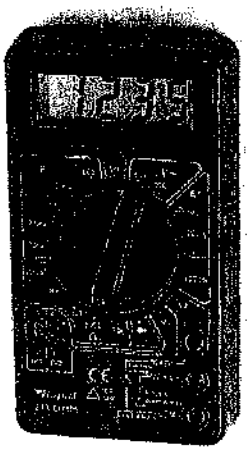


Figure 4.10: Digital Multimeter.

If we are using an analogue multimeter, make sure it has a high sensitivity of 20 KW/V or greater on DC voltage ranges, anything less is not suitable for electronics. The sensitivity is normally marked in a corner of the scale, ignore the lower AC value (sensitivity on AC ranges is less important).

All digital meters contain a battery to power the display so they use virtually no power from the circuit under test. This means that on their DC voltage ranges they have a very high resistance (usually called input impedance) of 1M W or more, usually 10M W, and they are very unlikely to affect the circuit under test.

Typical ranges for digital multimeters like are
(the values given are the maximum reading on each range)

- DC Voltage: 200mV, 2000mV, 20V, 200V, 600V.
- AC Voltage: 200V, 600V.
- DC Current: 200µA, 2000µA, 20mA, 200mA.
- AC Current: None. (You are unlikely to need to measure this).
- Resistance: 200 W, 2000 W, 20k W, 200k W, 2000k W, Diode Test.
- Digital meters have a special diode test setting because their resistance ranges cannot be used to test diodes and other semiconductors.

Analogue multimeters

Analogue meters take a little power from the circuit under test to operate their pointer. They must have a high sensitivity of at least 20kW /V or they may upset the circuit under test and give an incorrect reading. Batteries inside the meter provide power for the resistance ranges, they will last several years but you should avoide leaving the meter set to a resistance range in case the leads touch accidentally and run the battery flat.

Typical ranges for analogue multimeters like are (the voltage and current values given are the maximum reading on each range)

- DC Voltage: 0.5V, 2.5V, 10V, 50V, 250V, 1000V.
- AC Voltage: 10V, 50V, 250V, 1000V.
- DC Current: 50μA, 2.5mA, 25mA, 250mA.

A high current range is often missing from this type of meter.

- AC Current: None. (You are unlikely to need to measure this).
- Resistance: 20 W, 200 W, 2k W, 20k W, 200k W.

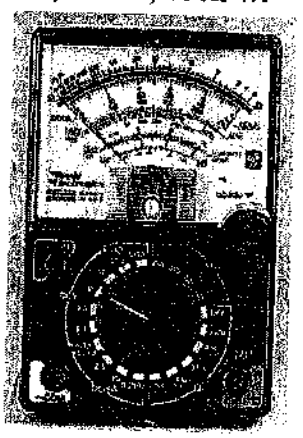


Figure 4.11: Analogue Multimeter.

These resistance values are in the middle of the scale for each range. It is a good idea to leave an analogue multimeter set to a DC voltage range such as 10V when not in use. It is less likely to be damaged by careless use on this range, and there is a good chance that it will be the range you need to use next anyway!

Sensitivity of an Analogue Multimeter

Multimeters must have a high sensitivity of at least 20k W/V otherwise their resistance on DC voltage ranges may be too low to avoid upsetting the circuit under test and giving an incorrect reading. To obtain valid readings the meter resistance should be at least 10 times the circuit resistance (take this to be the highest resistor value near where the meter is connected). You can increase the meter resistance by selecting a higher voltage range, but this may give a reading which is too small to read accurately!

On any DC voltage range:

Analogue Meter Resistance = Sensitivity × Max. reading of range

e.g. a meter with 20k W /V sensitivity on its 10V range has a resistance of 20k W/V×10V=200kW.

By contrast, digital multimeters have a constant resistance of at least 1M W (often 10M W) on all their DC voltage ranges. This is more than enough for almost all circuits.

Measuring voltage and current with a multimeter

1. Select a range with a maximum greater than you expect the reading to be.
2. Connect the meter, making sure the leads are the correct way round. Digital meters can be safely connected in reverse, but an analogue meter may be damaged.
3. If the reading goes off the scale: immediately disconnect and select a higher range.

Multimeters are easily damaged by careless use so we should take these precautions:

- Always disconnect the multimeter before adjusting the range switch.
- Always check the setting of the range switch before you connect to a circuit.
- Never leave a multimeter set to a current range (except when actually taking a reading)

The greatest risk of damage is on the current ranges because the meter has a low resistance.

4.11 HOUSE WIRING MATERIAL AND ACCESSORIES

The term wire is used more or less synonymously in house wiring. Strictly speaking, single wire, may be bare or covered with insulation is known as a wire and several wires stranded together is known as a cable. But in practice bare conductors, whether single or stranded together are termed as wire and conductor covered with insulation are termed as cables.

The necessary requirements of a cable are that it should conduct electricity efficient, cheaply and safely. This should neither be small so as to have a large internal voltage drop nor be too large so as to cost too much. Its insulation should be such as to prevent leakage of current in unwanted direction and thus to minimize risk of fire and shock. The cable consists of three parts:

(i) The conductor and core: The metal wire or strand of wires carrying the current.
(ii) The insulation or dielectric: a covering of insulating material to avoid leakage of current from the conductors and
(iii) The protective covering for protection of insulation from mechanical damage.

4.11.1 Type of Cables Used in Internal Wiring

The wires employed for internal wiring of buildings may be divided into different groups according to (i) Conductors used (ii) Number of cores used (iii) Voltage grading and (iv) Type of insulation used.

According to the conductor material used in cables these may be divided into two classes known as copper conductor cables and aluminum conductor cables.

According to the number of cores, the cable may be divided into classes known as single core cables: twin core cables, Tree core cables, two core with ECC (earth continuity conductor) cables etc.

According to the voltage grading the cables may be divided into two classes: (i) 250/440 volt cables and (ii) 650/1100 volts cables

According to type of insulation the cables are of the following types:

(i) Vulcanized Indian- Rubber (VIR) insulated cables
(ii) Tough rubber sheathed (TRS) or cab tire sheathed (CTS) cables.
(iii) Lead sheathed cables
(iv) Polyvinyl chloride (PVC) cables.
(v) Weather proof cables
(vi) Flexible cords and cables
(vii) XLPE cables

4.11.2 Conducit Accesserries

For conduct wiring system various accessories are required. The various accessories and fittings required for conduct wiring are described below.

4.11.3 Conduit Couplers

Conduit is available in lengths from 3 meters to 5 meters and for straight runs of greater length, couplers are used to join two lengths of conduct. The lengths of screwed conduits are always threaded at both ends on outer side. The threads on conduits are usually tapered. If shorter lengths are required then they must be cut of with a hack saw, all roughness removed from the end and threads with a die. One coupler is supplied free of cost with each length of conduit by manufacturer. The couplers are threaded on it's inner surface.

Figure 4.12: Rigid Condoit Coupling (Screwed).

4.11.4 Conduit Bushings

These are used when the rigid conduit enters the conduit box or a hole which is not threaded. These are used to prevent cable from being cut by the edges. These are made either from malleable iron or formed sheet steel. These are of two types male and female. Male bushes are provided threads on

either upper surface and female bushes are provided threads on either inner surface. Conduit can be directly screwed into the female type of bushes. Male bushes are used along with couplers. The coupler from outside and bush screwed in from inside of the box ensures electrical conductivity of the arrangement in addition to providing of a mechanically round conduit termination.

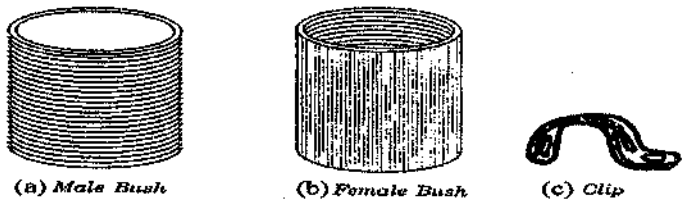


Figure: 4.13

4.11.5 Light Accessories

There are various types of light accessories e.g. switches, ceiling rose, socket-outlets, plugs and lamp holders are distributed below

(i) Switches:– A switch is used in an electric circuit as a device for making or breaking the electric circuit in a convenient way i.e. by the single motion of knob or handle to connect together or disconnect two terminals to which wires or cables are connected. This is the function of an ordinary single pole single way switch for switching lamps on and off.

(ii) Celling Rose:– The ceiling rose is used to connect the pendant lamps, fans or fluorescent tubes to installation through flexible plastic or silk covered wire.

4.12 TYPE OF WIRING

The type of internal wiring usually employed in our country are:

(i) Cleat wiring
(ii) Wooden casing and capping wiring
(iii) CTS or TRS or PVC sheathed wiring
(iv) Lead sheathed or metal sheathed wiring
(v) Conduit wiring
  (a) Surface or open type
  (b) Recessed or concealed or underground type

(i) Cleat Wiring:– In this system of internal wiring the cables used are either VIR or PVC type. The cables are held by porcelain cleats about 6mm above the wall or ceilings. The cleats are made in two halves, one base and other cap. The base is grooved to accommodate the cables and the cap is put over it and whole of it is then screwed on wooden plugs (gaieties) previously cemented into the wall and ceiling. Thus the cables are firmly gripped between the two halves of the cleats and secured to the supporting wall and ceiling. The screws used are of size 38 mm The cross-section of wooden gaieties used is 38mm × 38mm at big end, 25mm × 25mm at small end and length is about 6.5 cm. The cleats are used different size and different types in order to accommodate cables of various sizes and different numbers of cables of respectively.

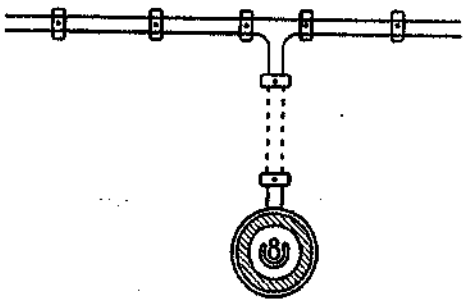


Figure 4.14: Cleat Wiring.

(ii) **Wooden Casing and Capping Wiring:**– The cables used in this type of wiring are either VIR or PVC or any other approved insulated cables. The cables are carried through the wooden casing enclosures. The casing consists of V-shaped grooves (usually two to hold the cables of opposite polarity in different grooves) and is covered at the top by means of rectangular strip of wood, known as capping of same width as that of casing. The capping is screwed to the casing by means of 13mmx4mm wooden screws fixed at every 15cm on the centre fitted. To protect the casing against white ants first class seasoned teak wood varnished by shellac varnish is employed. Two or three cables of same polarity (either all phases or all neutrals) may be run in the same groove. The casing is usually placed 3.2mm apart from the wall or ceiling by means of porcelain distance pieces of thickness not less than 6.5 mm in order to keep the casing dry at the back. The wooden gaieties on which the casing is screwed by means of 32mm × 8mm wooden screws are fitted into walls or ceilings at intervals not exceeding 90cm for sizes of casing capping up to 64mm and not exceeding 60 cm for sizes more than 64mm. The size of the casing capping to be used depends upon the number and size of cables to be accommodated in any particular length of run.

Figure 4.15: Wooden Casing.

(iii) **CTS or TRS Wiring:**– In this type of wiring the cables used may be single core twin core or three core TRS cables with a circular or oval shape. Usually single core cables are preferred. TRS cable are sufficiently chemical proof, water proof, steam proof but are slightly affected by lubricating oils. TRS cables are run on well seasoned, perfectly straight and well varnished (on all four sides) teak wood batten of thickness 10mm a least. The width of battens are available in width of 13,19,25,31,38,44,50,56,63,69 and 75mm. For guidance the number of copper conductor cable size 3/0.736 mm or aluminum conductor cables of size 1/1.40mm (usually used I internal wiring) can be carried by batten of different sizes. The wood battens are secured to the walls or ceilings by flat head wood screw to wood or other approved plugs at an interval not exceeding 75cm. The cables are held on the wood batten by means o tinned brass link clips already fixed on the batten with brass pins and spaced at a interval of 10 cm in case of vertical runs.

(iv) **Lead Sheathed or Metal Sheated Wiring:**– In this system of wiring, the cables used are insulated wires, TRS or PVC with an outer covering of sheath of lead-aluminum alloy containing about 95% lead. This metal sheath gives protection to the cable from mechanical injury, dampeners and atmospheric correction. The whole lead covering is made electrically continuous and is connected to earth at the point of outre to protect against electrolytic action due to leakage current and to provide safety against the sheath becoming alive. The cables are run on well seasoned and perfectly straight teak wood batten of thickness not less than 10mm and are fixed to it by means of links clips as in case of TRS wiring. The batten shall be well varnished with two coats at the back and the front small be painted with two coats of point of color to match the surroundings. The width of the wooden batten may be vary in accordance with the number of wires it may have to carry. The batten shall be run or brick walls, stone walls or plastered walls and ceiling steel joist or any structural steel work. The wood plugs for fixing the batten shall be of standard size as mentioned in general specifications and be placed at a distance of 75cm. The wood screw shall be used for fixing the batten. Only tinned brass clips of suitable size shall be used for fixing the cables on the well erected wooden batten.

(v) **Conduit Wiring:**– In this system of wiring steel tubes, known are conduit as installed on the surface of walls by means of saddles or pipe hooks or buried under plaster and VIR or PVC cables are drawn afterwards by means of a GI wire of size of about 18SWG. In dump situations the conduits can be spaced from the walls by means of small wooden blocks fixed below the pipes at regular intervals. In order to facilitate drawing of wiring number of inspection fittings are provided along its length.

4.13 BASIC PRINCIPLE OF EARTHING

All the metal parts of an appliance or an equipment which are supposed not to carry any current are to be earthed (i.e. to be connected to earth). This is known as earthling. This connection is made using a low resistance metal wire/ rod/ plate buried in the ground. The object of earthling is to ensure that a line to earth fault produces the same conditions as a short circuit between line and neutral cables.

4.13.1 Purpose of Earthing

An electric power system consists of major parts such as generators, transforms etc. To provide safety to those major parts of the system from lightening strokes and earth fault, it is necessary to provide earthing. This is termed as system earthing. For the safety of other equipments and the persons working with these equipments, it is necessary to provide earthing to the individual equipment. This is termed as equipment earthing. The purpose of earthing is twofold. First, to provide safety to operating persons and equipments by connecting the undesired potential to ground. Second to provide proper and reliable operation of protective equipment. This avoids results in reduction of maintenance of repair cost. Figure (4.16) explains how earthing provides safety. Here an appliance has been supplied electricity through 3-pin socket. The neutral and live terminals of the 3-pin socket have been connected to an electric supply system which is grounded.

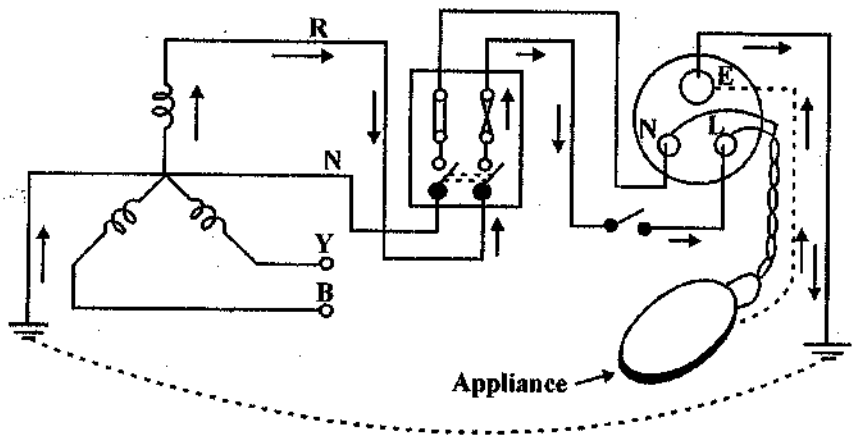


Figure 4.16: Earthing Provides Safety.

The third point of the 3-pin socket (earth point) has been connected to the metal part of the appliances. Whenever due to any reason the live wire comes in contact with the metallic body of the equipment, heavy current flows in the path as shown in Figure (4.16). This heavy current causes the fuse to blow off or the respective MCB to trip. This disconnects the faulty appliance from the supply. As it takes a very short time for the fuse to blow off or the MCB trip, no damage is cause to the appliance or to be installation. On the other hand if the appliance is not earthed and the fault as explained above occurs will cause the body of the appliance to be at line potential. Under these conditions any person working on the appliance is likely to get an electric shock as and when he touches the body of the appliance. In this way earthing provides safety to the equipment as well as to the person working on the appliance.

4.14 WIRING LAYOUTS FOR A COMPUTER LAB

The wiring closet adjacent to the computer facility is the central "hub" for the entire institute building. Therefore, the backbone from the main building is connected in the wiring closet in the computer facility. The computer lab will be designed and built so that the speed of the facility is 100 Mbps. It will be wired with category 5 unshielded twisted-pair cabling. Each computer in the facility comes Ethernet (100 BaseT) ready. The printers are either Ethernet ready or have a Jet Direct server to provide Ethernet capability. Two of the hubs for the facility, located in the wiring closet, will be 100 BaseT unmanaged hubs. These will connect the majority of the equipment that will be of the 100 BaseT variety. It can provide for 1 switchable 10/100 BaseT unmanaged hub for any 10 Base T equipment

that may be used or added to the room. The remainder of the building will actually connect through a backbone to the same wiring closet. The main point of entry or exit to the internet is through the equipment located in the Wiring Closet.

Internet connectivity is through the Internet Service Provider. Figure (4.18) illustrates the connectivity of the computer facility to the rest of the building and computer network connecting all computers and printers within the room.

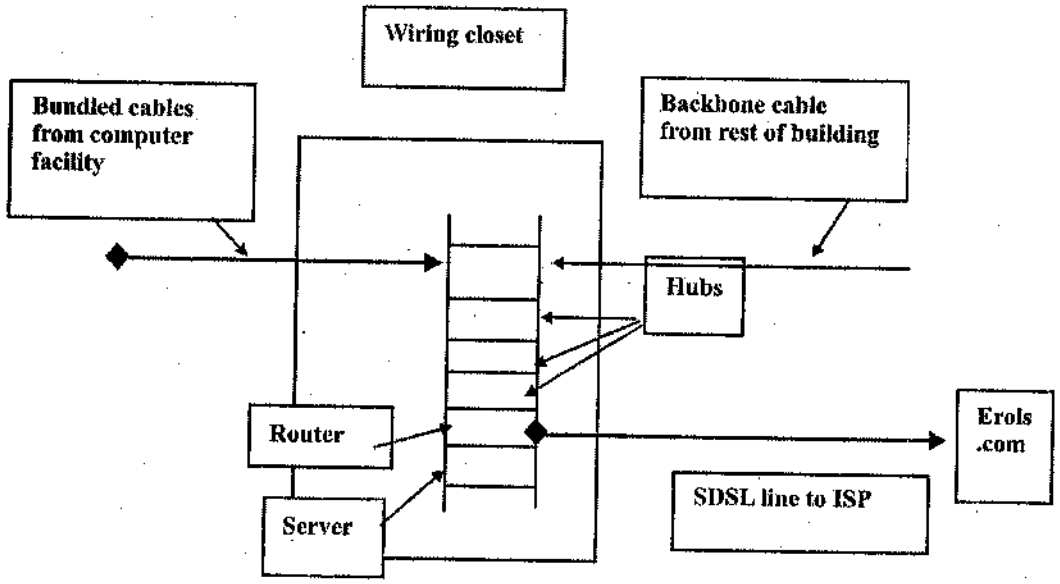


Figure 4.18: Wiring Layout for a Computer Lab.

4.15 SUMMARY

(1) D.C. generator can produce the value of emf (dc current or voltage) constant in magnitude and direction also.

(2) D.C. motors are used in daily life.

(3) Transformers is used in all a.c. operations. The cost of transmission is reduced considerably.

(4) Three phase systems are most commonly used in all modern generators.

(5) Home electrical wiring are an important tool for completing our electrical projects.

(6) Electrical wiring guide for the various phases of home electrical projects based upon function ality and safety for us and our family.

(7) Principal of earthing guided for the safety of instrument as well as humen's life.

4.16 REVIEW QUESTIONS

Q.1 What are the advantages of a three phase system over a single phase system?

Q.2 What is an ideal transformer? With the help of necessary diagram explain the working principle of an ideal transformer?

Q.3 Derive the emf equation of a single phase transformer and deduce the expression for trans former ratio?

Q.4 Explain why core of transformer is laminated?

Q.5 Briefly discuss the working principle of dc generator?

Q.6 Discuss the working principle of dc motor?

Q.7 Explain the significance of back emf in dc motor?

Q.8 Which quantity is measured by these measuring instruments:
(i) ammeter
(ii) voltmeter and
(iii) galvanometer

Q.9 What is multimeter? How it is measure current and voltmeter?

Q.10 What is the difference between wire and cable?

Q.11 Which insulation is most widely used for covering wires/cables used in internal wiring and

why?

Q.12 What for ceiling rose is used?

Q.13 What is earthing? Explain the purpose of earthing?

Q.14 Why earthing is essential?

Q.15 What are the insulating materials, that are used in cables?

Unit-05
SEMICONDUCTORS

Content of the Unit

5.0 OBJECTIVE

In this chapter we will discuss –

- The discovery of semiconductors replaced the vacuum tubes as they are small in size, operate at low voltage, consume very small power, having long life and high reliability.
- The semiconductor junction led to the discovery of integrated circuit which have revolutionized the electronic industry as they have been used in the working of television and computer which are very commonly used in our daily life.
- In this chapter we shall learn the basic concepts of semiconductors and their applications.

5.1 INTRODUCTION

The branch of physics which deals with the semiconductors is known as semiconductor physics. Certain materials are neither good conductor nor insulator, their conductivity lies between conductors and insulators, these materials are classified as semiconductors (*i.e.* Germanium, Silicon, Carbon etc). All most all electronic devices (i.e. diode, transistor, FET, OPAMPS etc.) are made up of semiconductors. Therefore, to study their characteristics and behavior, we should be familiar with the basic physics of semiconductor.

5.2 MOBILITY

A crystal lattice contains large number of free electrons which move randomly only at room temperature, therefore, number of electrons crossing the area of crystal in any direction will be same as the number of electron moving in opposite direction. So the net amount of current carried by electron is cancelled out and hence no current is set up in the crystal.

But under the influence of applied electric field, the charge carriers are accelerated parallel to the direction of applied electric field. In their movement these free electrons collide with the other electrons or with ions. There is a loss of energy in each collision. This give rise to electrical resistivity of semiconductors. The average distance between two successive collisions is the mean tree path and the time spent in travelling through this distance is called mean free time (τ).

In steady state condition the rise in kinetic energy of electron is balanced with the increase in energy loss due to collision. In this state net kinetic energy of electrons become constant and electrons move with a finite steady velocity which is called drift velocity. Drift velocity of electrons lie in the range of $(10^{-3} - 10^{-5})$ m/see.

The drift velocity (V) is directly proportional to intensity of applied electric field (E). The constant of proportionality is called mobility (m), and has a unit of cm^2/Volt-sec.

$$V = \mu E$$

$$\mu = \frac{V}{E}$$

Mobility is related to mean free time(τ) by the following relation.

$$\mu = \frac{e\tau}{m}$$

Where m, is the mass of electron (i.e. 9.1×10^{-31} kg). Mobility of conduction electrons is more than valence electrons, since conduction electrons are more easily affected than valence electrons. (Valence band is inner band of atoms where influence of applied electric field is least). Current carried by valence electrons is termed as hole current. So the mobility of holes is lower than conduction electrons. Mobility of charge carriers are zero at 0 K.

5.3 CONDUCTIVITY

A well known electrical property of a material is its resistivity ρ and given by the relation

$$\rho = \frac{RA}{L}$$

where 'R' is the resistance, 'A' is cross section area and 'L' is length.
Reciprocal of resistivity (ρ) is called electrical conductivity (σ) and its unit is mho/m

$$\Rightarrow \qquad \sigma = \frac{1}{\rho} = \frac{L}{RA}$$

Mathematically it is expressed as $\sigma = ne\mu$

Where n = number of charge carriers per unit volume (*i.e.* concentration)
μ = mobility of charge carriers
e = electric charge on charge carriers
= 1.6×10^{-19} C (for electron and hole)

5.3.1 Conductivity for Intrinsic Semiconductor

Intrinsic semiconductor is bipolar in nature i.e. it has both electrons and holes as charge carriers. So conductivity is

$$\sigma = n_e e \mu_e + n_h e \mu_n$$

Where n_e and n_n are number densities of intrinsic carriers i.e. electrons and holes or μ_e and μ_n are motilities of electrons and hole respectively.

5.3.2 Conductivity For Extrinsic Semiconductor

Extrinsic semiconductor, P type has majority of charge carriers as holes and in N- type semiconductor, electrons are majority charge carriers.

For P- type semiconductor $n_n > n_e$

$$\sigma = n_n e > \mu_n$$

For N- type semiconductor $n_e > n_n$

$$\sigma = n_e e > e\mu_e$$

At 0 K, mobility of electrons and hole is zero, so conductivity will be zero and semiconductor behaves like insulator at 0K.

5.4 ELECRONS AND HOLS IN AN INRINSIC SEMICONDUTOR

Germanium and Silicon are the two most important semiconductors used in electronic devices. Silicon has a total of 14 electrons in its atomic structure. Each atom in a Silicon crystal contributes four valence electrons, so that the atom is tetravalent. The inert ionic core of the Si atom carries a positive charge of + 4 measured in unit of the electronic charge. As Si has four electrons in outer shell, each electron is shared by neighboring atom and hence covalent bond is formed. This covalent bond is represented in Figure (5.1).

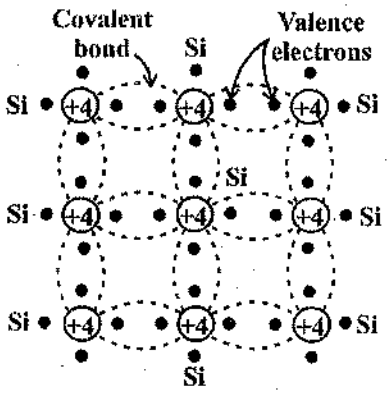


Figure 5.1: Crystal structure of Si.

At very low temperature 0K the Ge crystal behaves as an insulator, since no free carriers of electricity are available. But at the room temperature some covalent bonds are broken. Thermal energy required to break the bond is 1.lev for Si and 0.72ev for Ge at room temperature. The absence of electron in the covalent bond is represented by the small circle in Figure (5.2) and such an incomplete covalent bond is called a hole.

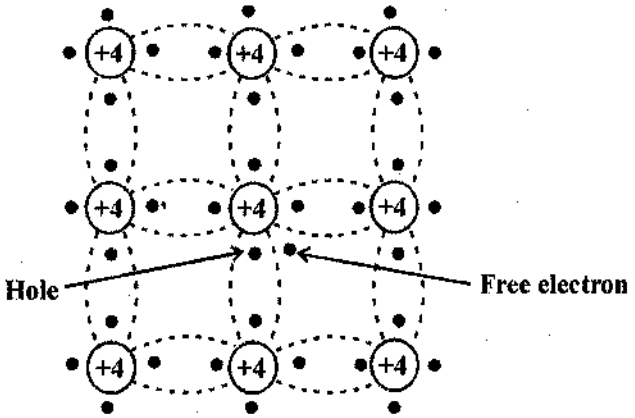


Figure 5.2: Si Crystal with a broken covalent bond.

i.e. the removal of electron leaves a vacancy, which is shown in Figure (5.2) by a small circle. This small circle which is a hole act as a positive charge for one electron set free one hole is created. Therefore, due to thermal energy pairs of electron and hole are created, there being as many holes as the free electrons. Here we have a current carrying mechanism of hole.

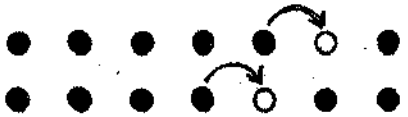


Figure 5.3: Mechanism of flow of hole.

Assuming that a hole exists in a covalent bond. Electron from neighboring atom fills this hole and leaves a hole at its own position. This process will continue. Valence electron move towards right and it appears as holes are moving towards lift. Basically current carried by valence electrons in valence band is said to be the hole current and current carried by free electrons in conduction band is termed as electron current. So far as the flow of electric current is concerned, the hole behaves like a positive charge equal in magnitude to the electronic charge.

In a pure (Intrinsic) semiconductor the concentration of holes (n_h is equal to the concentration of electrons n_e)

$\Rightarrow \quad n_e = n_h = n_i$ where n_i is called intrinsic concentration.

5.5 ELEMENTARY PROPERTIES OF GERMANIUM AND SILICON

Germanium and silicon are the important examples of intrinsic semiconductor which are widely used in electronic and transistor manufacturing. A pure Ge atom has 32 electrons and Si atom has 14 electrons

Silicon (14) $1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^2$

Germanium (32) $1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^6\ 3d^{10}\ 4s^2\ 4p^2$

Both the atoms have thus four valence electron. The crystal structure of Ge in two dimensions is shown in Figure (5.4).

The four valence electrons of a germanium atoms form four covalent bonds by sharing the electrons of neighboring four germanium atoms. Each covalent bond shares two electrons one from each atom. By forming such covalent bonds each Ge atom in the crystal behaves as if the outermost orbit of each atom is complete with eight electrons, having no free electrons in the Ge structure.

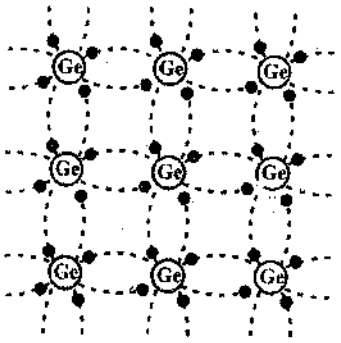


Figure 5.4: Two dimentional crystal structure of Ge.

At temperature 0K for the Ge structure the valance band is all full. The energy gap is 0.72ev and the conduction band is totally empty as shown in Figure (5.5) Since no electron is available for conduction therefore, the Ge crystal at 0K acts as electrical insulator. The conduction is possible if some of the electrons break away from their covalent bonds and become free. The minimum energy required to break a covalent bond is 0.72ev for Ge and 1.1ev for Si.

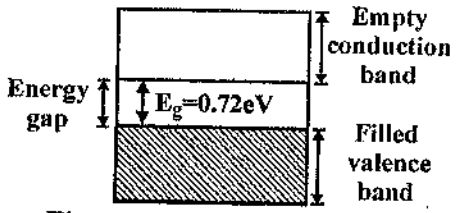


Figure 5.5: Ge crystal at 0 K.

Even at room temperature, the thermal vibrations of the atoms provide energy to the electrons in valence band to enable some electrons cross the forbidden gap and enter into the conduction band as free electrons, accounting for some electrical conductivity of the semiconductor. Higher is the temperature, larger will be the number of electrons crossing over the conduction band leaving behind equal no. of holes in the valence band.

5.6 DONOR AND ACCEPTOR IMPURITIES

If trivalent or pentavalent impurities are added to intrinsic semiconductor a doped, impure or extrinsic semiconductor is formed.

Trivalent impurities – B, Al , Ga, In , Tl

Pentavalent Impurities – N, P As, Sb, Bi

Doners – These are substances which have five valence electrons (Pentavalent), four electrons form covalent bond with atoms of intrinsic semiconductor and fifth is loosely bound.

The energy required to detach this fifth electron from the atom is 0.01ev for Ge and 0.05ev for Si. This low amount of energy is very easily available at room temperature. Sutable pentavalent impurities are antimony, phosphorus and arsenic. Such impurities donate excess electron (negative) carriers and so this type of semiconductor is known as N – type semiconductor,

Since every pentavalent atom donate one electron it is also called Donor Impurity. Addition of donor impurity creates new acceptable energy level (E_D) in the forbidden energy gap, it lie just below conduction band. Energy level is only (0.01ev) for Ge and 0.05ev in Si. This low level energy is available at room temperature, so all donor electrons jump from donor level to conduction level quite easily and large number of free electrons are available, this increasing the conduc-

tivity.

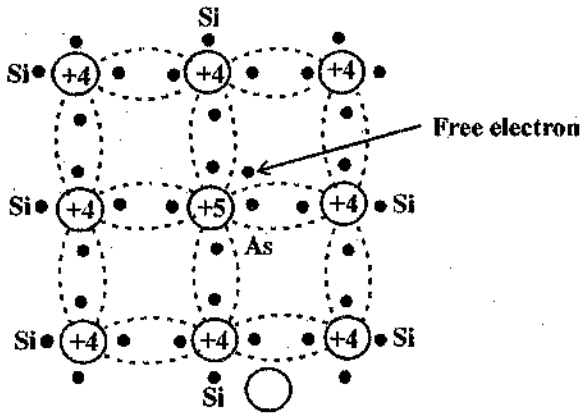


Figure 5.6: N-Type extrinsic semiconductor.

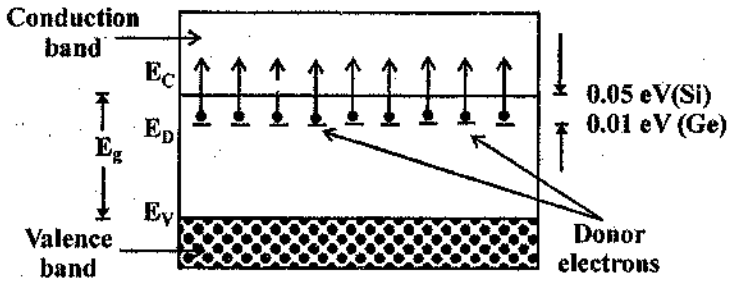


Figure 5.7: Effect of donor impurities on energy band structure.

Acceptor Impurities:– If a trivalent impurity (boron, gallium or indium) is added to an intrinsic semiconductor only these of the covalent bonds can be filled and the vacancy that exists in the fourth bond constitutes a hole. This is shown in Figure (5.8). Total number of holes in an extrinsic semiconductor depends upon number of added trivalent atoms. Since every trivalent atom accepts one electron so these type of impurities are known as acceptor impurities. Current conduction in P- type semiconductor is due to holes that have positive charge therefore acceptor impurities are called as P- type impurities and semiconductor so formed is called P-type semiconductor.

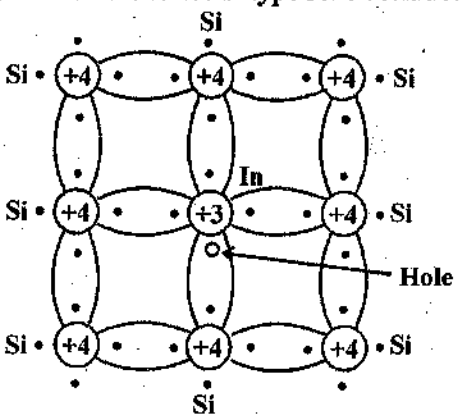


Figure 5.8: P-type semiconductor.

Figure (5.8) shows an acceptor impurity (Indium) added to Silicon. It produces new energy levels called acceptor energy level (E_A) in the forbidden energy gap. It lies just above the valence band as shown in Figure (5.9). These new energy levels contain holes. Electrons from valence band moves into acceptor level (E_A) and recombine with holes so they leave holes in valence band Figure (5.9). Hole is created at one point due to movement of electron from point 1 to acceptor level. Electron from point 2 jumped to point 1 and created hole at points 2. Therefore hole shifted from point 1 to point 2 opposite to direction of flow of electron. This shifting of points continues and movement of hole from point 1 to point 5 as shown in Figure (5.10).

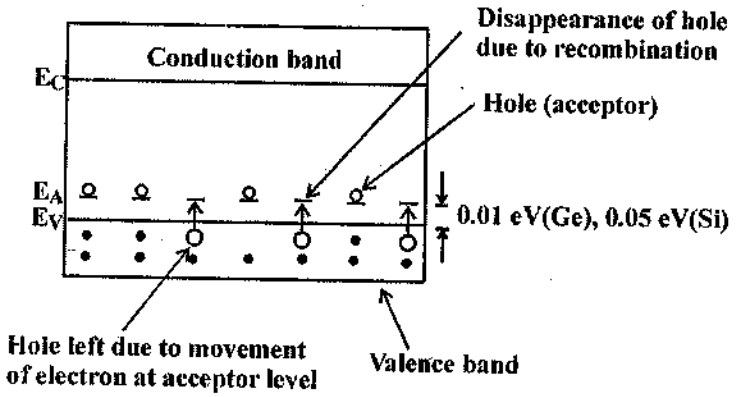


Figure 5.9: Energy band structure of acceptor impurity.

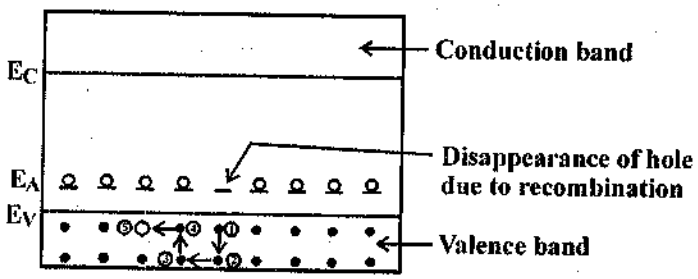


Figure 5.10: Movement of hole in valence band.

Therefore in P type semiconductors, the current conduction in valence band is due to valence electrons. Since it appears as holes are moving in valence band. So it is termed as whole current. Every acceptor atom acquires negative charge after accepting electron and called immobile negative ion.

5.7 GENERATION AND RECOMBATION OF CHARGES

In a pure semiconductor (intrinsic) the concentration of electrons and holes are always equal. Due to thermal agitation, new electron hole pairs are created, while at the same time other hole-electron pairs disappear due to recombination. Recombination is a process which free electrons (conduction electron) falls in to empty covalent bond (Hole). Before recombination, the electron–hole pair exist for some time. This time is called the mean life time. Mean life time vary in the range of 10^{-4} sec to 10^{-9} sec. Life time of hole and electron is indicated by τ_p and τ_n respectively.

When light falls on semiconductor, light photons impart their energy ($E = h\upsilon$) to bounded electrons and creates electron and hole pairs so electron and hole pairs can be created through temperature and photoelectric radiations.

Consider a bar of N- type silicon. Under steady state let the concentration of hole and electron be h_o and e_o. At the steady state condition the rate of generation becomes equal to rate of recombination. At instant t=to light falls on Silicon bar, addition hole electron pairs are generated uniformly throughout the crystal. Figure (5.11). After some time equilibrium state is reached again under the influence of light radiations. Let the new values of holes and electrons be n''_h and n''_e respectively.

$\Rightarrow$ Excess (or injected) holes = $h''_h - n_{no}$

and excess (or injected) electrons = $n''_e - n_{eo}$

since the light radiation creates equal number of hole electron pairs,

therefore $n''_n - n_{no} = n''_e - n_{eo}$

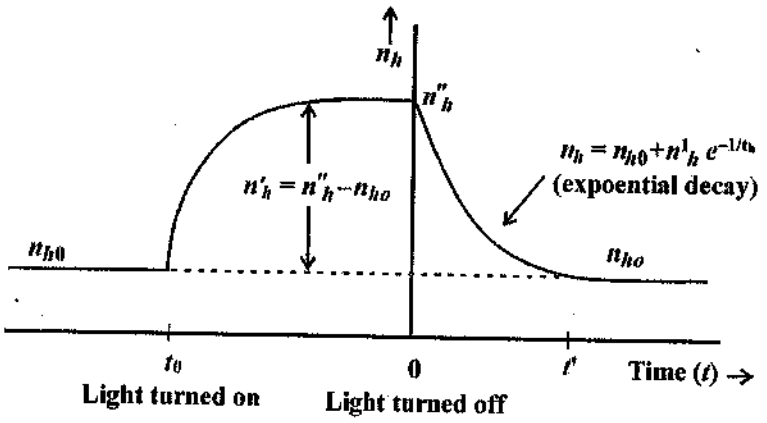


Figure 5.11: Variation of hole concentration with time in an N-type silicon bar.

As N- type Silicon bar contain large number of majority carriers (electrons) and negligible minority carriers (holes), therefore, percentage increase in concentration of electrons is negligible in comparison with holes. So, In other words we can say that radiation affects the concentration of minority carriers and concentration of majority carriers is hardly affected.

If light radiation continuously falls on semiconductor bar, the concentration of holes and electrons will be maintained constant at n_h and n_e respectively. But if radiations are removed, the excess charge carriers will recombine and their concentration will return to original steady state value h_o and e_o. The light radiation are removed at t=0 as shown in Figure (5.11). We will see that how excess minority carriers decay exponentially with time. We know that hole exists for a mean life time τ_h.

So decrease in concentration of holes per second due to recombination = $\frac{n_h}{\tau_h}$ ...(1).

At the same time holes are generated due to thermal energy. Let the generation rate be G.

Increase in concentration of holes per second due to generation = K .....(2)

Since charge can neither be created nor be destroyed so the rate of increase will be more than rate of decrease before thermal equilibrium reaches.

Let the net rate of increase of holes is $\frac{dn_h}{dt}$ then from equations (1) and (2) we have

$$\frac{dn_h}{dt} = K - \frac{n_h}{\tau_h} \qquad \ldots (3)$$

at t= t' again steady state reaches and the concentration of hole become constant (equal to h_0) therefore

$$\frac{dn_h}{dt} = 0 \qquad \ldots(4)$$

substituting in equation (3), we have

$$K = \frac{n_{h0}}{\tau_h} \quad (\text{at } t = t', n_h = n_{h0}) \qquad \ldots(5)$$

Substituting the value of K in equation (3) we have

$$\frac{dn_h}{dt} = \frac{n_{h0}}{\tau_h} - \frac{n_h}{\tau_h} = \frac{n_{h0} - n_h}{\tau_h} \qquad \ldots(6)$$

Where n_h indicates the net holes at any instant and n_{h0} is the concentration of holes under steady state without photo excitation. Let the excess holes at any instant is represented by n'''

$$n_h - n_{h0} = n'''_h \qquad \ldots (7)$$

Where n_h is the concentration of excess holes under steady state with light turned on and n'''_h is the concentration of excess holes at any instant.

Differentiating with respect to time

$$\frac{dn_n}{dt} = \frac{dn_n'''}{dt} \qquad \text{... (8) [} n_n''' \text{ is constant]}$$

substituting in equation (3), we have

$$\frac{dn_n'''}{dt} = \frac{n_{n0} - n_n}{\tau_n} = -\frac{n_n'''}{\tau_n}$$

$$\frac{dn_n'''}{dt} + \frac{n_n'''}{\tau_n} = 0 \qquad \text{... (9)}$$

This is a differential equation of first order. The solution o this equation is :

$$n_n''' = C_1 e^{-\frac{t}{\tau_n}} \qquad \text{... (10)}$$

at, $t = 0$ $\qquad n_h''' = n_h' = n_h'' - n_{h0}$ $\qquad$ ... (11)

(excess holes at t = 0 is equal to n_h''' Figure 5.11)

Substituting in equation 10 we have

$$C_1 = n_h'$$

$$\Rightarrow \qquad V = n_h' \; n_n''' e^{-\frac{t}{\tau_n}} \qquad \text{... (12)}$$

This equation indicates that excess charge carriers decay exponentially with time towards zero (at $t \to \infty$, $V \to 0$). As soon as the excess carriers die out, the concentration of charge carriers reaches its thermal equilibrium value (i.e. n_{h0} for holes and n_{e0} for electrons).

5.8 DIFFUSION

In metals the current is entirely drift current. Drift current flow due to application of external voltage. But in semiconductor an additional current is also present which is due to a mechanism called diffusion. Diffusion mechanism occurs in a gas container in which density of gas is not uniform. Gas particles travel from high density area to low density area. Similarly the charge carriers flow from highly doped area to lightly doped area in a nonuniformly doped semiconductor bar. This is called diffusion and current resulting from movement of charge carriers due to diffusion mechanism is called diffusion current.

Consider a nonuniformly doped P type semiconductor. Let us suppose that the concentration of holes(n_h) varies with distance x and concentration gradient is $\frac{dn_h}{dx}$.

Existence of concentration gradient causes movement of holes from highly doped area to lightly dope area (*i.e.* in x-direction). The current constituted by movement of holes is called hole diffusion currnt. The diffusion hole-current density (J_h) is proportional to concentration gradient hence

$$J_h \; \alpha \; \frac{dn_h}{dx}$$

$$\Rightarrow \qquad J_h = - \; q \; D_h \frac{dn_h}{dx} = - \; e \; D_h \frac{dn_h}{dx} \qquad \text{.... (1)}$$

(–ve sign is due to the fact that the slope $\frac{dn_h}{dx}$ is negative)

where

D_h = Difusion constant for holes

q = magnitude of charge of holes = e = 1.6×10^{-19} C

Similarly, the electron diffusion current density (J_n) is given by

$$\Rightarrow J_n = q \; D_n \frac{dn_e}{dx} \qquad = e \; D_n \frac{dn_e}{dx} \qquad \text{... (2)}$$

Negative sign is cancelled out, since charge 'q' is negative for electrons(i.e. q = –e)
Where D_n = diffusion constant for electron

In a semiconductor, it is possible that potential gradient and concentration gradient may exist simultaneously, therefore, existence of drift and diffusion current is possible simultaneously.
Total hole current density(J_h) is sum of current densities due to drift and diffusion, therefore, we have

$$J_h = n_h e \mu_n E - \frac{dn_h}{dx} D_n e \qquad \ldots (3)$$

Similarly total current density (J_n) is sum of electron drift current density and electron diffusion current density may occur in field free regions.

$$J_n = n_e e \mu_e E + \frac{dn_e}{dx} D_n e \qquad \ldots (4)$$

Drift current is a function of the electric field while diffusion current may occur in field free regions.

5.9 ENERGY BAND STRUCTURE OF OPEN CIRCUIT P-N JUNCTION

We know that the Fermi level (E_f) shows the probability of energy levels being filled. Rise in the level of E_f shows that electrons are occupying the higher energy levels. Similarly fall in the level of E_f shows the decrease in the energy content of electrons. In other words we can say that the Fermi level is an indication of average energy of electrons.
If P and N type semiconductor are joined together to form a diode, there would be transfer of electrons from one side of junction to another side till average energy of electron is again equal i.e. under the equilibrium the average energy of electrons of P and N region is equal. Since Fermi level (E_f) represents average energy of electrons, therefore, Fermi level of P and N rgion will at the same level. It is shown in Figure (5.12) where Fermi level of both sides line up.

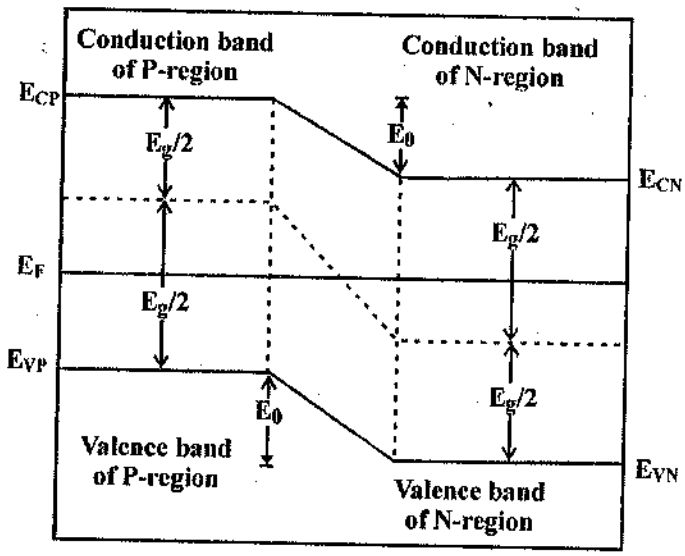


Figure 5.12: Energy band diagram of an open circuited P-N junction.

5.10 DEPLETION REGION

P-N junction can be formed by solid state diffusion or alloying. In alloying a 'dot' of P-impurity such as Indium is placed on substrate of N-type Silcon and this system is heated to high temperature and Indium fuses onto Silicon. On cooling down P-N junction is formed.

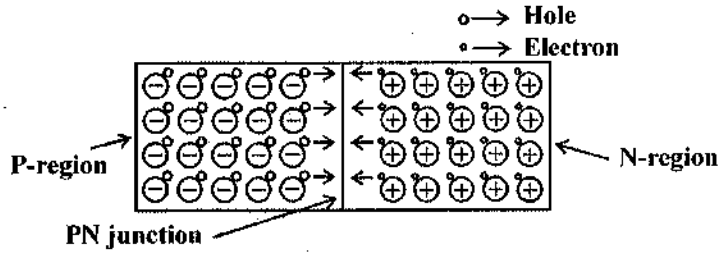


Figure 5.13: P-N Junction.

When a P-type semiconductor is suitably joined to N-type semiconductor, a new crystal is formed which is called diode and contact surface is called P-N junction and shown in Figure (5.13).

P-region has large concentration of holes and electrons are in minority. Similarly N-region contains large concentration of electrons and holes are in minority. Now because of density gradient across the junction free electrons move towards P-region and holes towards N-region. Movement of holes and electrons due to density gradient is called diffusion process Figure (5.13). When the free electron diffuses from N-region to P-region, it leaves behind an ionized donor on N-side. This ionized donor (positive charge) is immobile as it is bonded to the surrounding atoms. As the electrons continue to diffuse from N-region to P-region a layer of positive charge (or positive space-charge region) on N-side of the junction is developed. Similarly when a hoe diffuses from P-region to N-region due to density gradient, it leaves behind an ionized acceptor (negative charge) which is immobile. As the holes continue to diffuse a layer of negative charge (or negative space-charge region) on the P-side of the junction is developed. This space charge region on either side of the junction together is known as depletion region or space charge region. The thickness of the depletion region is of the order of one tenth of a micrometer.

When sufficient number of positive and negative ions are formed further diffusion prevented, now positive ions on N-side repel holes and negative ions of P-side repel free electrons. This barrier is called potential barriers.

5.11 SUMMARY

In this chapter the behavior of semiconductors are summarized as:

1. Two type of mobile charge carriers (positive holes and negative electrons) are available.
2. A semiconductor may be constructed with donor or accpto impurities.
3. At room temperature, essentially all donors and acceptors are ionized.
4. Current is due to two distinct phenomena, drift current and diffuse current.
5. The total majority carrier flow is the sum of a drift and a diffusion current.
6. Across an open circuited P-N junction there exist a contact diference of potential.

5.13 REVIEW QUESTIONS

Q.1 Explain the Mobility and conductivity ?

Q.2 Give the elementary properties of Ge and Si ?

Q.3 Differentiate between intrinsic and extrinsic semiconductors ?

Q.4 What do you understand by intrinsic and extrinsic semiconductor ?

Q.5 Distinguish between electrons and holes?

Q.6 Which semiconductor has more mobility: P-type or N-type ? Explain.

Q.7 Distinguish between N-type semiconductor and P-type semiconductor?

Q.8 What is "depletion layer" across the p-n junction?

Q.9 Explain drift and diffuse currents in semiconductor? Find expression for total electron current in a semiconductor?

Unit-06
PN JUCTION DIODE

Content of the Unit

6.0 OBJECTIVE

In this chapter we will discuss –

- In the study of semiconductor if a junction is formed between a sample of P-type and N-type semiconductor, this combination possesses the properties of a rectifier. P-N junction diode works in reverse wires as well as in forward wires.
- It is extensively used in electronic circuts due to its property of conducting current in one direction only.
- The volt-ampere characteristics of such a two terminal device (called a junction diode) is studied.
- In this chapter we shall study the properties, working and application of different types of junction diodes.

6.1 INTRODUCTION

The seed of the development of modern solid state semiconductor electronics goes back to 1930's when it was realized that some solid state semiconductor and their junctions of the possibility of cotrolling the number and the direction of flow of charge carriers through them. A P-N junction is the basic semiconductor device like diode, transistor etc. A clear understanding of the junction behaviour is important to analyse the working of other semiconductor device.

When a P- type semiconductor is suitably joined to N- type semiconductor, a new crystal is formed which is called P-N junction. P-N junction can be formed by solid state diffusion or alloying. In solid state diffusion, a impurities of one type (either P or N) are diffused into the body doped with opposite type of impurity at an appropriate high temperature.

In alloying a 'dot' of P- impurity such as Indium is placed on substrate of N-type Silicon and this system is heated to high temperature and Indium fuses on to Silicon. On cooling down P-N junction is formed.

6.2 P-N JUNCTION AS A RECTIFIER

When P-N junction diode act as a rectifier it permits the easy flow of charge in one direction but restrains the flow in opposite direction . Now we will consider qualitatively how this P-N junction diode behave as rectifier.

(1) REVERSE BIASING

Figure (6.1 a) shows the rectifire symbol of P-N junction diode in reverse bias. The negative terminal of the Battery is connected to the P-side and positive to N-side of the P-N junction. Positive terminal of the battery attracts electron from N-side and due to movement of the electrons away from the junction, more As shown in the above Figure (6.1a) the negative terminal of the Battery is connected to the P-side and positive to N-side of the P-N junction. Positive terminal of

the battery attracts electron from N-side and due to movement of the electrons away from the junction, more donor atoms are uncovered and become positive ions.

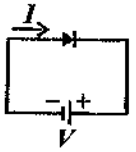


Figure 6.1: (a) The Rectifire Symbol is used for P-N Junction Diode.

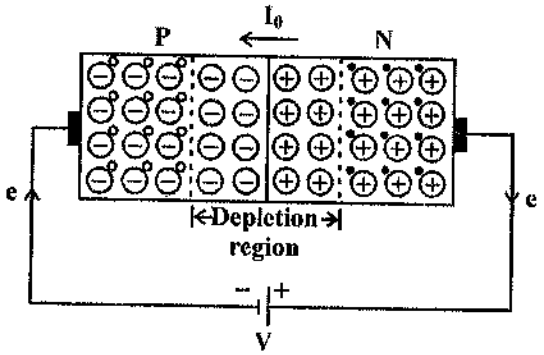


Figure 6.1: (b) Reverse biased P-N Junction

Similarly negative terminal attracts holes from P- side, so that holes move away from the junction. As holes leave acceptor atoms, these atoms acquire negative charge and become negative immobile ions. Since negative and positive ions increases in number, therefore thickness of depletion layer and contact potential increases. The greater the reverse bias, the wider the depletion layer becomes. The depletion layer stops growing when contact potential becomes equal to potential of biasing battery. As barrier potential increases with increase in reverse bias, therefore, majority carriers (holes in P- side and electrons in N-side) could not cross the junction. As a result, the current due to majority carriers will be zero. The P-N junction offers very high resistance under reverse bias.

As holes in N-type and electrons in P- type are minority carriers. So potential of N-side in depletion region is more than the potential of P- side, therefore the direction of electric field will be from N-side to P- side. This electric field helps the minority carriers in crossing the junction. Holes of N- region move in the direction of electric field and cross the junction similarly the electrons of P- region move opposite to the direction of electric field and cross the junction. As electron moves from P- region to N- region and holes move from N- region to P- region therefore a current will flow whose direction is from N region to P region Figure (6.1 b).

Current constituted by minority carriers under reverse bias condition is called minority current and denoted by I_0. This minority current depend only upon the temperature and independent of applied reverse voltage. For a particular fix temperature, minority current (I_0) reaches its maximum value quickly and does not change with increase in reverse bias potential i.e. it is also called reverse saturated current. It is of the order of microampere for Ge and nanoampere for Si.

(2) FORWARD BIASING

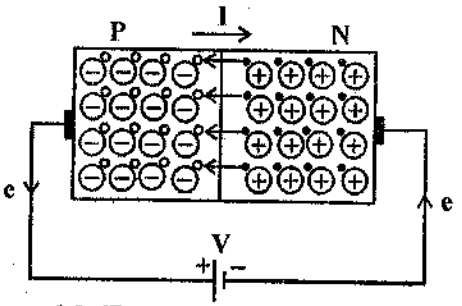


Figure 6.2: Forward biased P-N Junction.

P-N junction diode is said to be forward biased when P- side of diode is connected with positive terminal of battery and N-side of diode is connected by negative terminal of battery as shown in Figure (6.2). Negative terminal of battery repel electrons of N-side towards the junction i.e. electrons moves

in to depletion region and merged with positive ions reconverts positive ions in to neutral donor atoms. Similarly holes are repelled by positive terminal of battery and they merge with negative ions and neutralize them. As the concentration of positive and negative ions decreases depletion width decreases and finally it completely disappears when applied forward voltage is equal to cut in potential.

Now majority charge carriers (holes in P-side diode and electrons in N-side diode) can cross the junction and they constitute a large current which is called forward current. It is directed from P to N region. The junction offers low resistance in there forward biased junction.

6.3 CURRENT COMPONENTS OF A P-N DIODE

When P-N junction diode is forward biased, holes from the P-side enter the N-side. Similarly, electrons from the N-side move into the P-side. This process is called minority carries injection. A forward biased diode is shown in Figure (6.3 a). Holes are injected from P-side to N-side and electrons from N-side to P-side. Density of injected carriers are maximum at junction at $x = 0$ and decrease exponentially with distance x due to recombination as shown in Figure (6.3 b) up to the end of the surface almost all injected minority carriers recombine with majority carriers (i.e. injected holes recombine with electrons in the N- side and injected electrons recombine with holes in P-side). Therefore at the end of N region the concentration of holes is equal to natural concentration n_{ho}. similarly for P-region the number of electrons at the end of the surface will be equal to natural or intrinsic concentration n_{eo}. If doping of P and N-region are different, then concentration of injected holes and electrons will be different. In Figure (6.3 b) P-region is considered as highly doped and N-region as lightly doped (i.e. $n_h^{"} > n_e^{"}$). Highly doped region has lower concentration of intrinsic minority carriers (i.e $n_{ho} > n_{eo}$).

The current in diode is carried by injected holes and electrons. Since N-region lightly doped the current due to electrons can be neglected and it can be considered that the current flow is only due to injected holes and it is given by

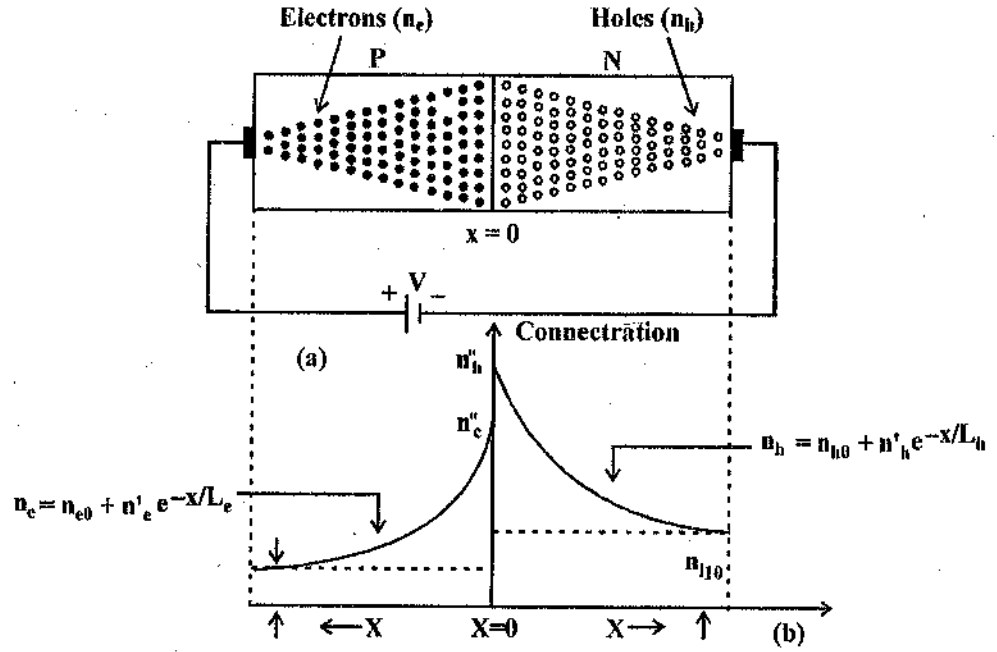


Figure 6.3: (a) Forward biased Diode (b) Minority carrier density distribution

$$I = \frac{AqD_h n'_h}{L_h} \qquad \ldots (1)$$

Where $q = 1.6 \times 10^{-19}$ c,

L_h = diffusion length of holes

A = Area of cross section

n_h' = no. of holes injected in N-region at x=0

$$n_h' = n_h^* - n_{ho}$$

$$Q = AqL_h n_h' \qquad \ldots (2)$$

From equation (1) and (2) we get

$$\frac{Q}{I} = \frac{L_h^2}{D_n} = C$$

$$I = \frac{Q}{C} \qquad \ldots (3)$$

Where τ is the mean life time of hole

$$\tau = \frac{L_h^2}{D_n} \qquad \ldots (4)$$

Equation (3) states that diode current is proportional to the stored charge of excess minority carriers.

6.4 IDEAL VOLTAGE AMPERE CHARACTERISTICS

For a P-N junction the current I is related to the Voltage V by the given equation.

$$I = I_0 \left[e^{\frac{V}{\eta V_T}} - 1 \right] \qquad \ldots (1)$$

When the current flows from P-Side to N-Side in the diode then the value of I is positive. Here V_T is the volt equivalent of the temperature and is given by

$$V_T = \frac{KT}{q} = \frac{T}{11{,}600} \qquad \ldots (2)$$

Where K= Blotzmann constant = 1.381×10^{-23} Joule per Kalvin

q = electronic charge = 1.6×10^{-19} c

T = absolute temperature in Kelvin at room temperature (T = 300 K)

V_T = 26 mv

The value of η is unity for germanium and is approximately two for silicon. I_0 is known as the reverse saturation current, which is very small.

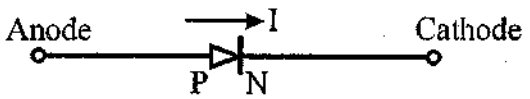
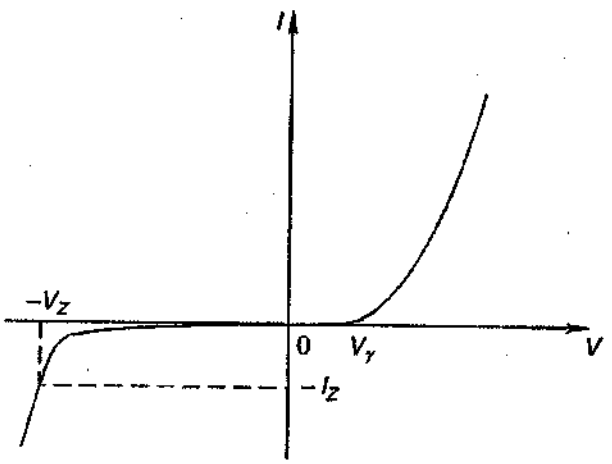


Figure 6.4: Symbolized Diode



Figrue 6.5: V - I Characteristics of a Semiconductor diode.

A diode is symbolized as shown in Figure (6.4) Where P-side is known as anode and N-side is known as cathode. Arrow indicates the direction of flow of current. The form of the voltampere

characteristics described by equation (1) is shown in Figure (6.5).

From the characteristics curve when P-N junction is forward biased, the potential barrier decreases and no appreciable current flow till forward voltage equal to break point threshold voltage or cut in potential (V_γ). The value of V_γ is approximately 0.2V and 0.6V for germanium and silicon diode respectively. Beyond the voltage V_γ the current rises very rapidly due to majority carriers (*i.e.* forward current) rises exponentially as defined by volt-ampere equation.

When P-N junction diode is in reverse biased movement of majority carriers are opposed. Although minority carriers can easily move and cross the junction but the concentration of these minority carrier is independent of reverse voltage, therefore a constant current (I_0) flows as shown in Figure (6.5). This is known as reverse saturation current (I_0). From Voltampere equation when V is negative (reverse voltage), the current through diode is

$$I = I_0\left[e^{\frac{V}{\eta V_T}} - 1\right]$$

$I = -I_0$ (Since exponential term is negligible in comparison to unity)

Thus we see that the diode is a unidirectional device i.e. it allows the current to flow in the forward diction (conducting) and does not allow the current to flow in the reverse direction (non–conducting) and hence acts as a switch.

The following important points may be summed up from the V-I characteristics.

(i) There is no flow of diode current at zero external voltage

(ii) At forward bias, the current increases slowly till the potential barrier is crossed.

(iii) The forward current rises abruptly after the knee voltage.

(iv) The forward current is limited by the value of series and junction resistances.

(v) The diode can be destroyed if the forward current exceeds the rated value.

(vi) At reverse bias, reverse current increases slightly with the increase in voltage due to minority carriers.

(vii) If reverse voltage is increase beyond the safe limit the reverse current rises abruptly due to breaking of the junction.

(viii) The reverse voltage at which the junction breaks is called breakdown voltage and the diode is destroyed at this voltage.

6.5 TEMPERATURE DEPENDENCE OF THE V/I CHARACTERISTICS

The temperature dependence of the volt ampere characteristic is important in many applications of diodes.

Temperature affects the V-I characteristics in following manner :

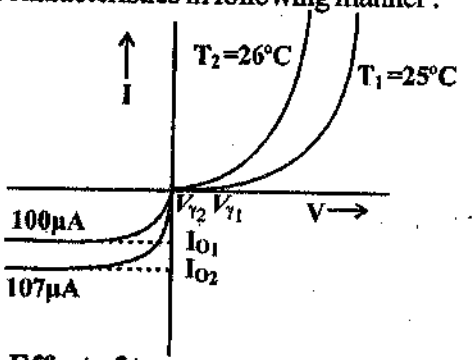


Figure 6.6: Effect of temperature on V-I characteristics.

(1) Reverse saturation current increases approximately 7% per degree for both Si and Ge *i.e.* it approximately double for every 10°C rise in temperture. If reverse saturation current is I_0 at T_1, then at T_2 it will be $I_{02} = I_{01} 2^{\frac{(T_2 - T_1)}{10}}$

(2) Contact potential (V_γ) decreases by 2.5 mV per degree rise in temperature *i.e.*

$$\frac{dV}{dT} = -2.5\ \text{mV}/^{0}C$$

These effects can be shown in Figure (6.6).

Above Figure (6.6) shows the V-I characteristics at two different temperature (25°C and 26°C).

Change in temperature $\Delta t = 26 - 25 = 1^{0}C$.

Let cutting volage at 25°C, V = 0.7V

Therefore cut in voltage at 26°C, $V_{\gamma_2} = 0.7 - 2.5 \times 10^{-3} \times \Delta t$

$= 0.7 - 2.5 \times 10^{-3} \times 1 = 0.6975$ V

It suggests that V-I characteristics shifts towards left with increase in temperature.

6.6 DIODE RESISTENCES

An ideal P-N junction diode has zero resistance in forward biasing and infinite resistance in reverse biasing, but practical diode is different from ideal diode. It offers finite low resistance (*i.e.* forward resistance R_f) of the order of few ohms in forward direction and very high resistance (R_r) of the order of mega ohms in the reverse directions. There are two types of diode resistances, static and dynamic resistance.

(1) Static Resistance:

Resistance offered by a diode to the d.c. conditions is called dc or static resistance. It is simply the ratio of dc voltage across diode to dc current through diode.

In forward region the static resistance is equal to reciprocal of the slope of a line joining operating point to the origin. Figure (6.7).

Static Resistance $R_f = \frac{V_D}{I_D}$

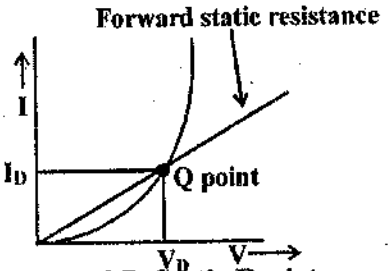


Figure 6.7: Static Resistance.

(2) Dynamic resistance

Resistance offered by diode to the ac conditions is called dynamic resistance of the diode. Dynamic resistance is defined as the ratio of change in applied voltage to the change in resulting current Figure (6.8).

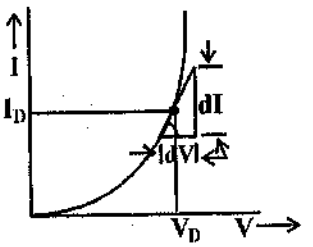


Figure 6.8: Dynamic Resistance.

Dynamic resistance $R_d = \frac{dV}{dI}$

In volt-ampere characteristics of diode the dynamic resistance is reciprocal of slope of tangent at that point.

6.7 JUNCTION DIODE SWITCHING TIMES

When a diode is turned ON and turned OFF, it will take finite time for both action i.e. a diode can neither turn on nor turn off instantly or in other words we can say that diode has two switching

time.Turn on time (Forward recovery time) and Turn off time (Reverse recovery time). In turn on time the voltage across diode (is in forward biased) is reduces. It is the time interval in which voltage across diode changes from maximum to minimum voltage. Figure (6.9 a).

In turn off time, the diode biasing is changes suddenly from forward to reverse biases, current does not drop to zero instantly. It takes finite time to reduce to zero this is known as Turn off time.

When a diode is forward biased, holes of P- region cross the junction and enter in to N-region. In N-region holes behave as minority carriers similarly electrons behave as minority carriers in P-region.

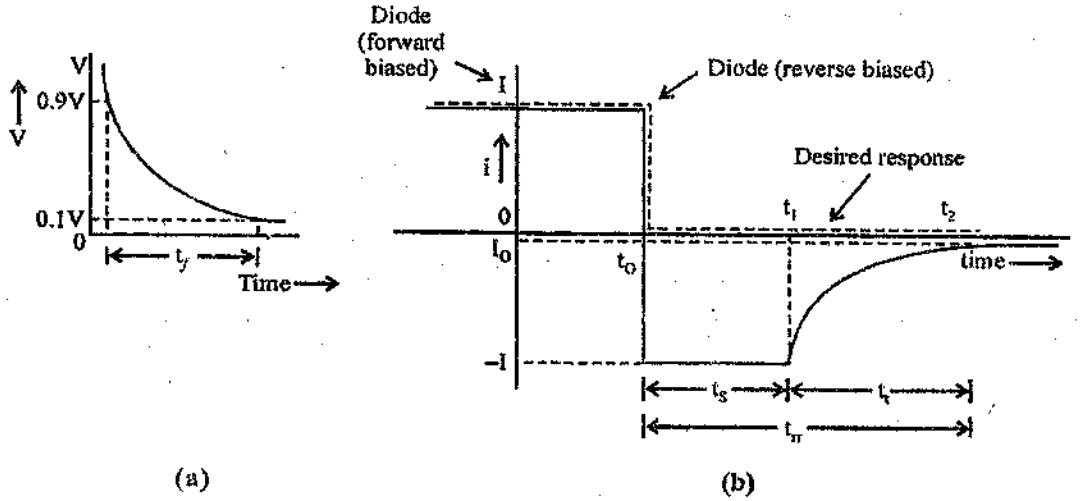


Figure 6.9: (a) Forward Recovery Time , (b) Reverse Recovery Time.

At $t = t_0$ Figure (6.9 b), the diode is suddenly reverse biased. But at this instant minority carriers are trapped in P and N regions. As potential energy barrier does not oppose the movement of minority carriers therefore they constitute minority current in reverse direction. The diode is still conducting so it is not returned to cut off stage. Therefore to turn off the diode, the injected minority carriers should be returned back to their parent regions i.e. electrons to N-region and holes to P-region. After returning back to their parent region, they behave as majority carrier and their movement is opposed by potential energy barrier and current drops to nearly zero and diode is turned off. If the diode is reverse biased, the biasing battery forces the minority carrier to return to their parent region, means to say that reverse biasing helps in turning off the diode.

When the diode is reverse biased injected minority holes and electrons are repels with the positive and negative terminal of the battery, i.e. a current flow from N-region to P-region (reverse current). This current is constant till all injected holes and electrons come back to their parent regions P and N region. This time internal ($t_1 - t_0$) is called storage time (t_s). After this event current falls to reverse saturation current (I_0). Reverse saturation current (I_0) is due to thermally generated minority carriers.

The time interval ($t_2 - t_1$) is called as transition time 't_t' as shown in Figure (6.9 b).

Sum of these two time internals (t_s and t_t) equals the turn off time or reverse recovery time (t_{rr}) of diode.

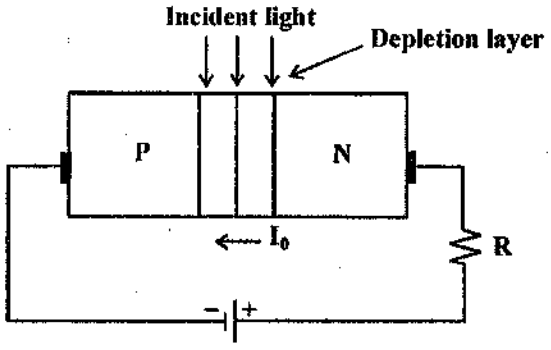
So turn off time $t_{rr} = t_s + t_t$

For the fast switching from ON state to OFF state, the t_{rr} should be as small as possible.

6.8 SEMICONDUCTOR PHOTODIODE

Semiconductor or P-N junction diode is a simple diode which is in reverse biased with a battery of voltage V. In this diode the current in reverse bias depend upon the intensity of light falling on P-N junction Figure (6.10).

In Semiconductor photo diode under normal condition a reverse saturation current (I_0) flows due to thermally generated minority carriers. This current does not depend upon the applied reverse voltage (reverse voltage opposes the flow of majority carriers and diffusion of minority carriers is unaffected). Minority carrier concentration depend upon temperature, therefore, reverse saturation current is a function of temperature.



Figyure 6.10: Photo Diode.

When light falls at the surface of P-N junction diode, light photons impart their energy to valence electrons to break the covalent bond so that additional electron hole pairs are generated. The concentration of electron hole pairs depends upon the energy of photons (*i.e.* the intensity of light). Due to these additionally generated electron hole pairs the total quantity of minority carriers increases. Thus increasing the reverse saturation current and the total reverse saturation current $I = I_0 + I_L$ where I_0 is due to thermally generated minority carriers and I_L is due to photo generated minority carriers. As I_L is a function of light intensity so reverse saturation current (I) of semiconductor photo diode depends upon intensity of light.

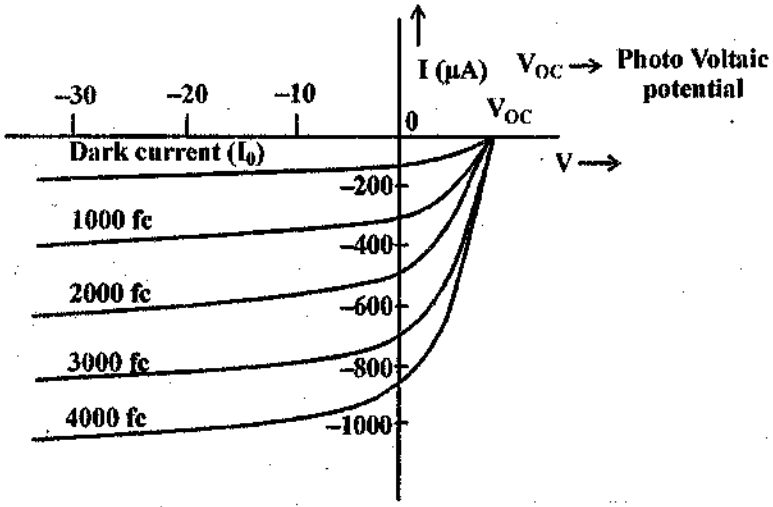


Figure 6.11: V-I Characteristics of Semiconductor Photo Diode.

Typical photo diode Volt-ampere characteristics have following features:

(i) Current with no light falling on junction is called dark current (I_0). It is a function of temperature only.

(ii) The curves (dark current curve) do not pass through the origin.

(iii) Reverse current is independent of amount of reverse voltage but increases with increase of intensity of light.

(iv) Magnitude of reverse current also depends upon distance of point of light falling from junction. Larger is the distance lesser will be the current.

Photo diode has following applications:

(i) Light detection system

(ii) Counting of objects

(iii) Reading of film sound trade

(iv) Light operated switches

(v) High speed reading of computer punched cards

(vi) Alarm System

6.9 PHOTO VOLTAIC EFFECT

We see that in semiconductor photodiode the reverse current due to minority carriers remains almost constant for large reverse voltages. Now if a forward voltage is applied, the forward current

due to majority carriers flow opposite to reverse current, therefore, magnitude of resultant current flowing through photodiode decreases. When this majority current equals to minority current, the total current is reduced to zero. The forward voltage at which resultant current is zero is called the photovoltaic potential. Under the open- circuited conditions no current flow, certainly the photo voltaic e.m.f. is obtained across the open terminal of a semiconductor junction. Photovoltaic cells are used to power electronic equipment to charge auxiliary storage batteries.

6.10 LIGHT EMITTING DIODE

Light emitting diode is a diode that can emits light when a current passes through it in forward direction. It is a useful device. It can emit light is different colours like red, green, yellow, orange and white.

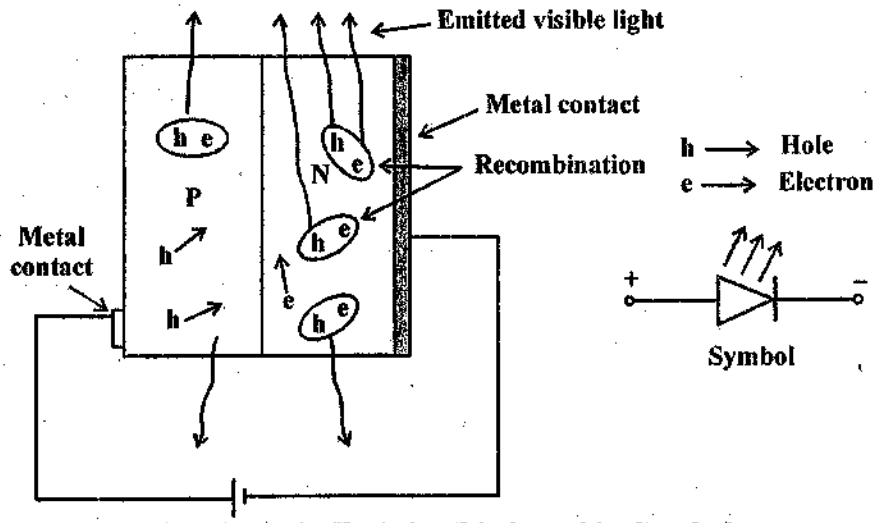


Fig 6.12 Light Emitting Diode and its Symbol.

LED is a simple P-N junction diode. It is made up of gallium arsenide (GaAS) or gallium phosphide (GaP). In these semiconductors a considerable amount of recombination takes place under these conditions the energy released when an electron falls from the conduction band in to the valence band appears in the form of radiation. So LED is a direct band gap type diode.

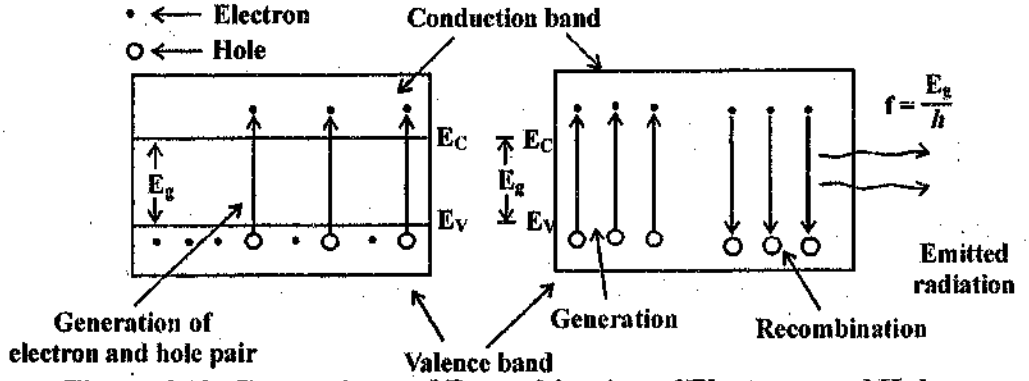


Figure 6.13: Generation and Recombination of Electrons and Holes.

When electron is excited from valence band to conduction band, the electron hole pair are created as shown in Figure (6.13). Electron stay in conduction band for a very short period ($\approx 10^{-9}$ sec) and then return back. In transition from higher energy state (conduction band E_c) to lower energy state (valence band E_v) these electrons release energy.

Energy released $E_g = E_c - E_v$

Frequency of radiation $f = \frac{E_g}{h}$

where, h is Planck's constant.

In silicon and germanium semiconductor this energy is given off in the form of heat and emitted light is negligible but in other material as gallium arsenide (GaAs), gallium phosphide (GaP) the number of

photons of light energy is sufficient and their frequency lie in visible range, therefore, light is visible in light emitting diode (LED).

The intensity of light depends upon the number of recombination which is proportional to the forward current in the diode Therefore intensity of light depends upon forward current through diodes. LED has following applications:

(1) LED is used in LASER diode and find application in optical communication system and in CD player.
(2) LED is used as an opto–isolator
(3) It is used in display devices.

6.11 SUMMARY

From all above discussion we conclude this chapter as follows

(1) The P-N junction can be considered to be equivalent to a capacitor with P and N regions acting as the plates of a capacitor and depletion region as the dielectric medium.
(2) In P-N junction there is a diffusion of majority carriers across the junction in forward biasing and driting f charge carriers in reverse biasing.
(3) An ideal diode offers zero resistance in forward direction and infinite resistance in reverse direction.
(4) For a fixed current, minority current (I_0) reaches its maximum value quickly and does not change with increase in reverse bias potential, therefore, it is called as reverse saturation current.
(5) Diode is a unidirectional device.
(6) The volt-ampere characteristics shifts towards left with increase in temperature.
(7) Diode (P-N junction) works the fast switching from ON state to OFF state.
(8) Reverse recovery time plays a major role in high speed switching application. For fast switch ing from ON state to OFF state the should be as small as possible.
(9) Intensity of light depends upon forward current through diodes.
(10) Light emitting diodes (LED) is used in opt-isolator and display devices.

6.12 REVIEW QUESTIONS

Q.1 What is a P-N junction? Explain the formation of potential barrier in a P-N junction?
Q.2 Discuss the behaviors of a P-N junction under forward and reverse biasing?
Q.3 Draw and explain the V-I characteristics of a P-N junction?
Q.4 Write short notes on the following : (1) Break down voltage (2) Knee voltage (3) Limitations in the operating conditions of P-N junction
Q.5 Explain the phenomena of photovoltaic effect?
Q.6 What is a light emitting diode?
Q.7 Describe semiconductor photodiode?
Q.8 (a) Draw the volt –ampere characteristics of a P-N photodiode?
(b) Does the current correspond to a forward or reverse biased diode.

Unit- 07
APPLICATIONS OF PN JUCTION DIODE

Content of the Unit

7.0 OBJECTIVE

In this chapter we will discuss –

- Use of PN-junction Diode as a Rectifier
- Design and Operation of Half Wave and Full Wave Rectifiers
- Design and Operation of Smoothing Filters
- Use of Zener Diode as regulator
- Design and Operation of Voltage Regulators.
- Switch Mode Power supply (SMPS) and advantage of SMPS over Linear Power Supply (LPS)

7.1 INTRODUCTION

Alternating current is preferred for generation, transmission and distribution means because of small losses, convenience and low cost. But, almost all electronic circuits need a DC power source. Batteries are used for power supply in portable device. More frequently, however, it is economical and convenient to draw DC power from a DC power supply. A piece of equipment which converts

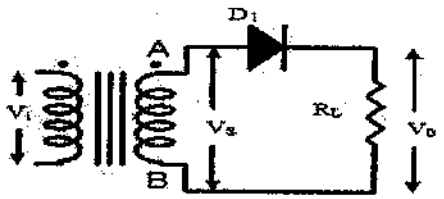


Fig. 7.1 (a) Half Wave Rectifier

Figure: 7.1 (a) Half wave rectifier.

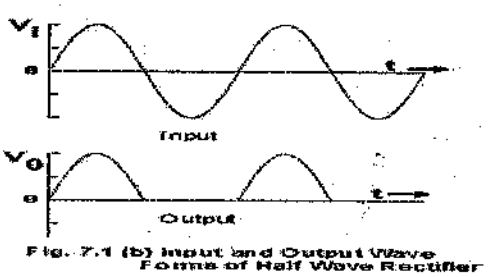


Fig. 7.1 (b) Input and Output Wave Forms of Half Wave Rectifier

Figure: 7.1 (b) Input and output wave forms of Half wave rectifier.

alternating voltage/current to direct voltage/current is known as **Rectifier**. The process of conversion of AC voltage/current to DC voltage/ current is known as **Rectification.**

Voltage or current received from the rectifier is unidirectional but its value changes with time. The output voltage and current of the rectifier is pulsating. The pulsating voltage can be considered as the sum of alternating and direct voltages. The circuits/devices which remove the ac component from the pulsating voltage are known as **smoothing Filter**.

Output DC voltage of power supply changes with the change in load. For a good power supply the output voltage should not change with the load. The circuits/device, which removes the dependence of output voltage on load, is known as **Regulators**.

7.2 P-N JUNCTION AS A RECTIFIER

A rectifier uses a unidirectional conduction device or asymmetrically conduction device. In Unidirectional conduction devices the device conducts only in one direction e.g. PN junction diode, while in asymmetrical conduction device, device conduct unequally in two directions. A PN junction diode is a unidirectional device. It offers small resistance (a few tens of ohms) in forward bias condition and large resistance (few kilo ohms) in case of reverse bias condition.

Rectifiers are two types, (i) **Half Wave Rectifier,** which conducts during one half of the applied AC voltage and, (ii) **Full Wave Rectifier,** which conducts for full wave of the applied AC voltage.

7.2.1 Half-Wave

Circuit diagram of half wave rectifier is shown in Figrue (7.1 a). In this circuit, an alternating voltage source is connected across the primary coil of a transformer and a PN junction diode and a load resistance is connected in series across the secondary coil of the transformer.

Let an alternating voltage $V_i = V_p \sin(\omega t)$ is applied across the primary coil of the transformer. If n is the ratio of the number of turn in secondary coil to number of turns in primary coil .Then $Vs = n V_p \sin \omega t$ will induce across the secondary coil of the transformer. For the positive half cycle of the input alternating voltage , end A of the secondary coil of the transformer will be at positive voltage and end B will be at negative voltage. Thus, PN junction diode will be forward biased and diode will conduct. There will be voltage drop ($V_0 = IR_L$) across the load R_L. While, for the next half cycle, end A will be at negative voltage and end B will be at positive voltage. This will reverse bias the PN junction diode and no current will flow across the load R_L. Input and Output Wave forms of half wave rectifier is shown in Fig.(7.1 b).

Let R_f be the forward bias resistance of the diode and R_s be the resistance of the secondary coil of the transformer. Then current across the load Resistance will be –

$$\left.\begin{aligned} I &= \frac{V_S}{R_L + R_f + R_S} = \frac{nV_p \sin \omega t}{R_L + R_f + R_S} \\ I &= I_m \sin \omega t \end{aligned}\right\} \quad \text{when } 0 < t < \frac{T}{2}$$

$$I = 0 \qquad \text{when } \frac{T}{2} < t < T$$

where $I_m = \dfrac{nV_p}{R_L + R_f + R_S} = \dfrac{V_m}{R_L + R}$

and $V_m = nV_p$ *and* $R = R_f + R_S$

Current (I) is unidirectional current but its magnitude is varying with time. Thus average pulsating current with respect to time will be

$$I_{dc} = \frac{1}{T}\int_0^T I\,dt = \frac{1}{T}\int_0^{\frac{T}{2}} I\,dt + \frac{1}{T}\int_{\frac{T}{2}}^{T} I\,dt$$

$$= \frac{I_m}{T}\int_0^{\frac{T}{2}} \sin\omega t\,dt = \frac{I_m}{\omega T}\left(-\cos\omega t\right)_0^{\frac{T}{2}}$$

$$= \frac{I_m}{\pi}$$

Similarly, the root mean square current (I_{rms}) will be –

$$I_{rms} = \sqrt{\overline{I^2}}$$

$$I_{rms}^2 = \frac{1}{T}\int_0^T I^2\,dt = \frac{1}{T}\int_0^{\frac{T}{2}} I^2\,dt + \frac{1}{T}\int_{\frac{T}{2}}^{T} I^2\,dt$$

$$= \frac{I_m^2}{T}\int_0^{\frac{T}{2}} \sin^2\omega t\,dt = \frac{I_m^2}{T}\int_0^{\frac{T}{2}} (1-\cos 2\omega t)\,dt$$

$$= \frac{I_m^2}{T}\left[t - \frac{\sin 2\omega t}{2\omega}\right]_0^{\frac{T}{2}} = \frac{I_m^2}{4}$$

7.2.1.1 Ripple Factor

Remaining pulsation in output voltage or current is known as Ripple. Effective ripple with respect to DC component is a measure of smoothing of the output voltage. Ratio of ripple component to dc component of output voltage or current is known as ripple factor.

$$r = \frac{\text{Effective value of output AC Component}}{\text{Average or output DC Component}}$$

Let I_{ac} be the effective output AC component and output DC component is I_{dc} then –
Total power across load = Power of DC component + Power of AC component

$$I_{rms}^2 R_L = I_{dc}^2 R_L + I_{ac}^2 R_L$$

$$I_{rms}^2 = I_{dc}^2 + I_{ac}^2$$

$$I_{ac}^2 = I_{rms}^2 - I_{dc}^2$$

$$I_{ac} = \sqrt{I_{rms}^2 - I_{dc}^2}$$

$$\text{Ripple factor} = \frac{I_{ac}}{I_{dc}} = \frac{\sqrt{I_{rms}^2 - I_{dc}^2}}{I_{dc}} = \left[\frac{I_{rms}^2}{I_{dc}^2} - 1\right]^{\frac{1}{2}}$$

$$= \left[\frac{I_m^2}{4}\cdot\frac{\pi^2}{I_m^2} - 1\right]^{\frac{1}{2}} = \left[\frac{\pi^2}{4} - 1\right]^{\frac{1}{2}}$$

$$= 1.21 = 121\%$$

Thus, in half wave rectifier AC component of current is more than the average value of DC current.

7.2.1.2 Efficiency

Ratio of output DC power to Input AC power is known as the efficiency of the Rectifier.

$$\text{Efficiency of Rectifier } \eta = \frac{\text{Output DC Power}}{\text{Input AC Power}} \times 100\ \%$$

$$= \frac{P_{dc}}{P_{ac}} \times 100\ \%$$

$$= \frac{I_{dc}^2 R_L}{I_{rms}^2 (R_s + R_f + R_L)} \times 100\% = \frac{I_{dc}^2 R_L}{I_{rms}^2 (R + R_L)} \times 100\%$$

$$= \frac{I_m^2}{\pi^2} \cdot \frac{4}{I_m^2} \cdot \frac{R_L}{(R + R_L)} \times 100\%$$

$$= \frac{4}{\pi^2} \cdot \frac{R_L}{(R + R_L)} \times 100\ \%$$

$$\eta = \frac{40.6}{\left(1 + \frac{R}{R_L}\right)}\ \%$$

i.e. maximum efficiency of half wave rectifier is 40.6 %

7.2.1.3 Voltage Regulation

Output DC voltage (V_{dc}) across the load $R_L = I_{dc} R_L$

It is clear from above equation that the output DC voltage V_{dc} depends upon load R_L. Percentage voltage regulation is defined as follows:

$$\text{Percentage Voltage Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\ \%$$

where V_{NL} = Open circuit output voltage, i.e.,output voltage in absence of load R_L

V_{FL} = Output voltage in presence of load R_L

For an ideal voltage source percentage voltage must be zero. For a half wave rectifier output DC voltage is given by

$$V_{dc} = I_{dc} R_L = \frac{I_m}{\pi} R_L$$

$$= \frac{V_m}{\pi (R + R_L)} R_L = \frac{V_m}{\pi} \left[1 - \frac{R}{R + R_L}\right]$$

$$= \frac{V_m}{\pi} - \frac{V_m}{\pi (R + R_L)} R$$

$$= \frac{V_m}{\pi} - I_{dc} R$$

When there is no load (R_L) present in the circuit then there will be no current in the circuit i.e. $I_{dc} = 0$.

Thus in this case voltage across the output terminal will be $V_{dc} = \frac{V_m}{\pi}$ which is equal to V_{NL}. Thus

$$VR = \frac{V_{NL} - V_{FL}}{V_{FL}}$$

$$= \frac{\frac{V_m}{\pi} - \left(\frac{V_m}{\pi} - I_{dc}R\right)}{\left(\frac{V_m}{\pi} - I_{dc}R\right)}$$

$$VR = \frac{I_{dc}R}{\left(\frac{V_m}{\pi} - I_{dc}R\right)}$$

7.2.2 Full-Wave Rectifiers

In full wave rectifier both (Negative and Positive) half cycle of input AC current is used. In this rectifier two similar PN junction diode (D_1 & D_2) are connected in the circuit as shown in the Figure (7.2 a). In this arrangement one diode conduct for first half cycle of input AC current while another one conduct for the second half cycle of the input AC current.

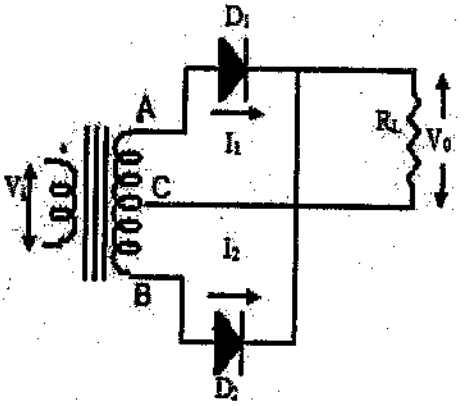


Fig. 7.2 (a) Full Wave Rectifier

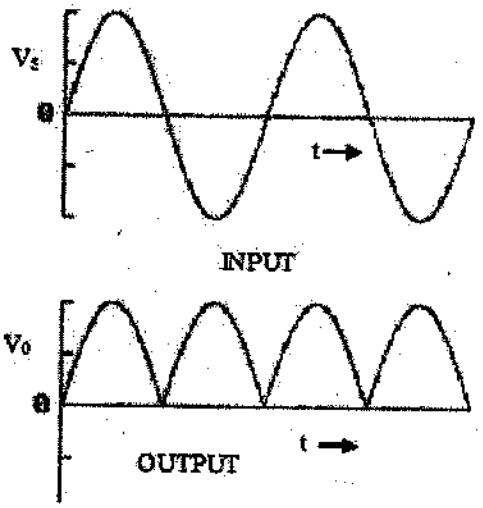


Fig. 7.2 (b) Input output Wave Forms of Full Wave Rectifier

An alternating voltage source $V_i = V_p \sin \omega t$ is applied across the primary coil of the central tapping transformer. End A and B of the secondary coil of the transformer are connected with P terminal of two PN junction diode D_1 & D_2 respectively. N terminal of both diode (D_1 & D_2) are connected together at a common point P. A load resistance is connected between common point P of diodes and center tap C of the secondary coil of transformer.

Let an alternating voltage $V_i = V_p \sin \omega t$ is applied across the primary coil of the transformer. If n be the ratio of the number of turn in secondary coil to number of turns in primary coil .Then $Vs = n V_p \sin \omega t$ will induce across the secondary coil of the transformer. For the positive half cycle of the input alternating voltage , end A of the secondary coil of the transformer will be at positive voltage and end B will be at negative voltage and center tap of the transformer C will be at zero potential. This will forward bias the D_1 diode and reverse bias the D_2 diode. Current I_1 will flow through the load R_L. While, in next negative half cycle of the input voltage end A will be at negative voltage and en B will be at positive voltage, which will reverse bias the D_1 diode and forward bias the D_2 diode. Current I_2 will flow throw the load R_L. As shown in the figure the direction of current will be same in both cases. Input and Output wave forms are shown in Figure (7.2b).

Let R_f be the forward bias resistance of both diodes (D_1 & D_2) and R_s be the resistance of the secondary coil of the transformer. Then current across the load resistance will be–

$$I_1 = \frac{V_S}{R_L + R_f + R_S} = \frac{nV_p \sin \omega t}{R_L + R_f + R_S}$$
$$I_1 = I_m \sin \omega t$$
$$I_2 = 0$$

when $0 < t < \frac{T}{2}$

$$I_1 = 0$$
$$I_2 = -\frac{V_S}{R_L + R_f + R_S} = -\frac{nV_p \sin \omega t}{R_L + R_f + R_S}$$
$$I_2 = -I_m \sin \omega t$$

when $\frac{T}{2} < t < T$

where $I_m = \frac{nV_p}{R_L + R_f + R_S} = \frac{V_m}{R_L + R}$

where $V_m = nV_p$ and $R = R_f + R_S$

and I_1, I_2 is the current through diode D_1 & D_2 respectively

Average pulsating current with respect to time will be

$$I_{dc} = \frac{1}{T}\int_0^T I\, dt = \frac{1}{T}\int_0^{\frac{T}{2}} I_1\, dt + \frac{1}{T}\int_{\frac{T}{2}}^T I_2\, dt$$

$$= \frac{I_m}{T}\int_0^{\frac{T}{2}} \sin \omega t\, dt - \frac{I_m}{T}\int_{\frac{T}{2}}^T \sin \omega t\, dt$$

$$= \frac{I_m}{\omega T}\left[(-\cos \omega t)_0^{\frac{T}{2}} - (-\cos \omega t)_{\frac{T}{2}}^T\right]$$

$$= \frac{I_m}{\pi}[2+2] = \frac{4I_m}{\pi}$$

The root mean square current (I_{rms}) will be -

$$I_{rms} = \sqrt{\overline{I^2}}$$

$$I_{rms}^2 = \frac{1}{T}\int_0^T I^2\, dt = \frac{1}{T}\int_0^{\frac{T}{2}} I_1^2\, dt + \frac{1}{T}\int_{\frac{T}{2}}^T I_2^2\, dt$$

$$= \frac{I_m^2}{T}\int_0^{\frac{T}{2}} \sin^2 \omega t\, dt + \frac{I_m^2}{T}\int_{\frac{T}{2}}^T \sin^2 \omega t\, dt = \frac{2I_m^2}{T}\int_0^{\frac{T}{2}} \sin^2 \omega t\, dt$$

$$= \frac{2I_m^2}{T}\int_0^{\frac{T}{2}} (1 - \cos 2\omega t)\, dt$$

$$= \frac{2I_m^2}{T}\left[t - \frac{\sin 2\omega t}{2\omega}\right]_0^{\frac{T}{2}} = \frac{I_m^2}{2}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

7.2.2.1 Ripple Factor

By definition ripple factor is given by -

$$r = \frac{\text{Effective value of output AC Component}}{\text{Average or output DC Component}}$$

$$\text{Ripple factor} = \frac{I_{ac}}{I_{dc}} = \frac{\sqrt{I_{rms}^2 - I_{dc}^2}}{I_{dc}} = \left[\frac{I_{rms}^2}{I_{dc}^2} - 1\right]^{\frac{1}{2}}$$

$$= \left[\frac{I_m^2}{2}\cdot\frac{\pi^2}{4I_m^2} - 1\right]^{\frac{1}{2}} = \left[\frac{\pi^2}{8} - 1\right]^{\frac{1}{2}}$$

$$= 0.482 \text{ or } 48.2\%$$

7.2.2.2 Efficiency

$$\text{Efficiency of Rectifier } \eta = \frac{\text{Output DC Power}}{\text{Input AC Power}} \times 100\ \%$$

$$= \frac{P_{dc}}{P_{ac}} \times 100\ \%$$

$$= \frac{I_{dc}^2 R_L}{I_{rms}^2 (R_s + R_f + R_L)} \times 100\%$$

$$= \frac{I_{dc}^2 R_L}{I_{rms}^2 (R + R_L)} \times 100\%$$

$$= \frac{4I_m^2}{\pi^2}\cdot\frac{2}{I_m^2}\cdot\frac{R_L}{(R+R_L)} \times 100\%$$

$$= \frac{8}{\pi^2}\cdot\frac{R_L}{(R+R_L)} \times 100\ \%$$

$$\eta = \frac{81.2}{\left(1 + \frac{R}{R_L}\right)}\ \%$$

i.e. maximum efficiency of full wave rectifier is 81.2%

7.2.2.3 Voltage Regulation

$$\text{Percentage Voltage Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\ \%$$

Where V_{NL} = Open circuit output voltage, i.e. output voltage in absence of load R_L

V_{FL} = Output voltage in presence of load R_L

For an ideal voltage source percentage voltage must be zero. For a Full wave rectifier Output DC Voltage is given by

$$V_{dc} = I_{dc}R_L = \frac{2I_m}{\pi} R_L$$

$$= \frac{2V_m}{\pi(R+R_L)} R_L = \frac{2V_m}{\pi}\left[1 - \frac{R}{R+R_L}\right]$$

$$= \frac{2V_m}{\pi} - \frac{2V_m}{\pi(R+R_L)} R$$

$$= \frac{2V_m}{\pi} - I_{dc}R$$

When there is no load (R_L) present in the circuit then there will be no current in the circuit i.e. $I_{dc} = 0$.

Thus in this case voltage across the output terminal will be $V_{dc} = \frac{2V_m}{\pi}$ which is equal to V_{NL}. Thus

$$VR = \frac{V_{NL} - V_{FL}}{V_{FL}}$$

$$= \frac{\frac{2V_m}{\pi} - \left(\frac{2V_m}{\pi} - I_{dc}R\right)}{\left(\frac{2V_m}{\pi} - I_{dc}R\right)}$$

$$VR = \frac{I_{dc}R}{\left(\frac{2V_m}{\pi} - I_{dc}R\right)}$$

7.3 FILTERS

The object of rectification is to provide a steady DC voltage, similar to the voltage from battery. We have seen in section 7.2.1 and 7.2.2 that the full wave rectifier is better rectifier in comparison to the half wave rectifier. But Full wave rectifier does not provide ripple-free dc voltage. Electronic equipment requires dc voltage of negligible ripple. So there is need to separate out the AC component from the output voltage of the rectifier. This process is known as **smoothing**. Circuits which perform the task of smoothing are known as **filters**.

There are many types of filter. Among them, a few important filters are as follows-

(i) Shunt Capacitor Filter
(ii) Series Inductor Filter
(iii) L-Section Filter
(iv) π-Section Filter

7.3.1 Shunt Capacitor Filters

Shunt capacitor filter is the cheapest and simplest filter. A capacitor C of large value is connected in shut with the load resistance R_L. Circuit diagram is shown in Figure (7.3a) and (7.3 b).

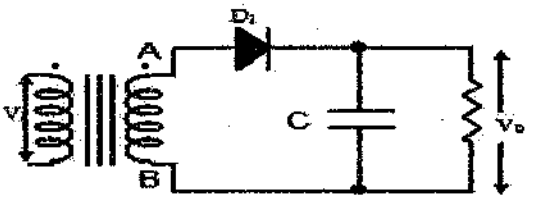


Fig. 7.3 (a) Half Wave Rectifier with Shunt Capacitor Filter

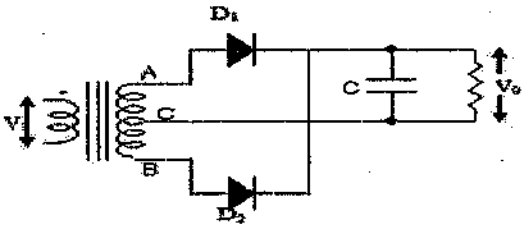


Fig. 7.3 (b) Full Wave Rectifier with Shunt Capacitor Filter

We know that the impedance of a capacitor is given by $X_C = \frac{1}{\omega C}$ and $\omega = 0$ for DC. Thus the capacitor C offers a low reactance path ($X_C < R_L$) to the AC component of output current of the rectifier while it will act as open circuit to the DC current. All DC current and a small AC component $\left(\frac{X_C}{X_C + R_L} I_{ac}\right)$ current will pass through the load R_L.

When the rectifier output is increasing the shunt capacitor charges to the peak voltage V_m and when rectifier output decreases from its peak value, capacitor C start discharging through load R_L and prevent load voltage from falling to zero. Wave form for full wave rectifier with shunt capacitance filter is shown in Figure (7.4). Ripple factor for full wave rectifier with shunt capacitance filter is -

$$\text{Ripple factor } r = \frac{0.144}{f R_L C}$$

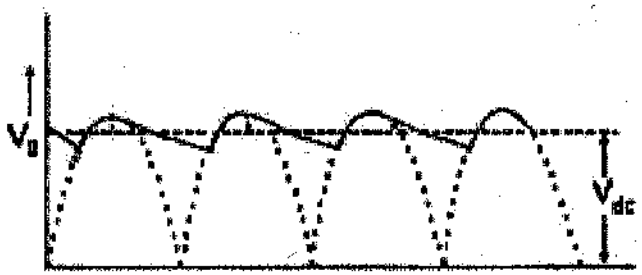


Figure 7.4 : Output wave form for full wave rectifier with shunt capacitance filter.

7.3.2 Series Inductor Filters

In this type of filter an inductor coil of high inductance is connected in series with the load R_L as shown in Figure (7.5 a) and (7.5 b). The working of series inductor coil is based on the fundamental property of opposing any change in current through of inductance coil. Whenever the current through inductor tend to change, an emf is induced across the inductance coil in such a way that it opposes the change in current.

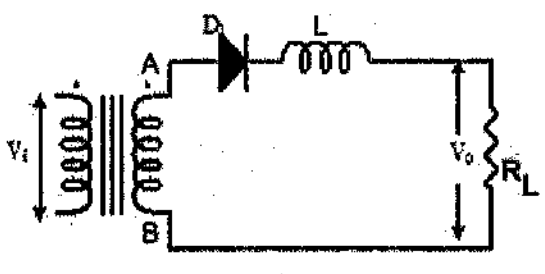


Fig. 7.5 (a) Half Wave Rectifier with Series Inductor Filter

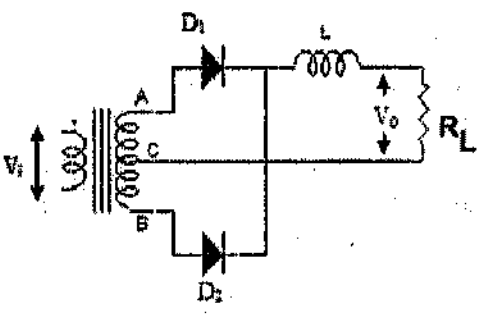


Fig. 7.5 (b) Full Wave Rectifier with Series Inductor Filter

We know that the impedance of an Inductor is given by $X_L = \omega L$. Thus an inductance coil will offer a high reactance path to the AC component present in the output current of the rectifier while it will offer zero reactance paths to the DC component of output current of rectifier.

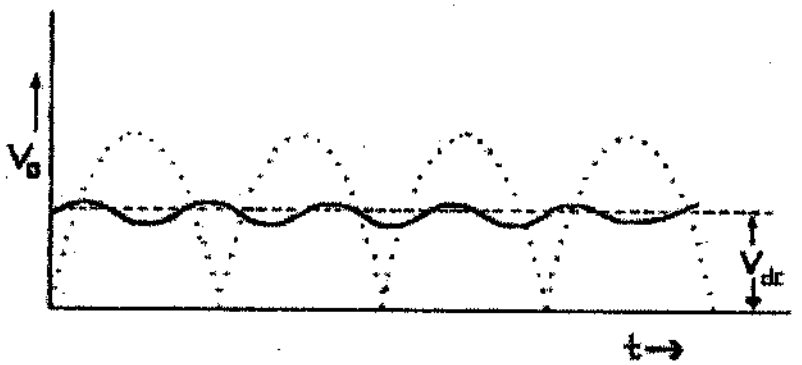


Figure 7.6: Output wave form for full wave rectifier with series iinductor filter.

When Output current of the rectifier increases and above the average value then it stores energy in the magnetic field and delivers the same energy to the load R_L when current reduces below the average value. Wave form for full wave rectifier with series Inductor filter is shown in Figure (7.6). Ripple factor for full wave rectifier with series Inductor filter is -

$$\text{Ripple factor } r = \frac{0.236}{\left(\frac{\omega L}{R_L}\right)}$$

7.3.3 L Section Filter or Choke Input Filter

Circuit diagram of L-section filter is shown in Figure (7.7 a) and (7.7b). In this circuit an inductor L is connected in series and apacitor C in shunt with load R_L. This name is due to the fact that inductor and capacitor are connected as an inverted L.

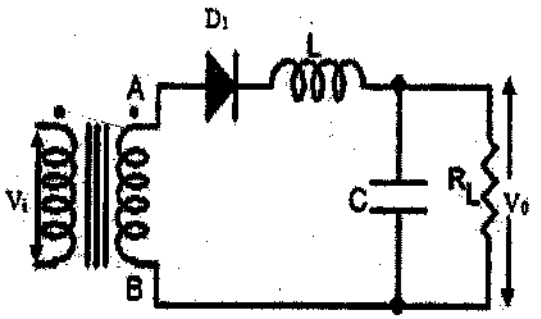


Fig. 7.7 (a) Half Wave Rectifier with L-Section Filter

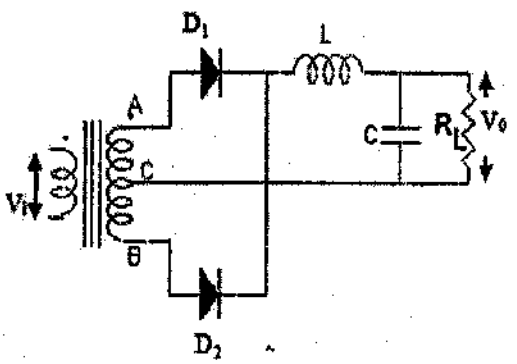


Fig. 7.7 (b) Full Wave Rectifier with L-Section Filter

In section 7.4.1 and section 7.4.2 we have seen that a series inductor filter passes the DC component from rectifier output but offer high impedance to the AC components. The AC component that remains after passing through L is passed through by shunt capacitor, which acts as open circuit to the DC component and provides low impedance path to the remaining AC component. In this way, a LC filter combines the features of both series inductor filter and shunt capacitor filter. Ripple factor for full wave rectifier with L section filter is –

$$\text{Ripple factor } r = \frac{0.118}{\omega^2 LC}$$

7.3.4 π Section Filter

π Section Filter consists of one inductor (L) and two capacitors (C_1 and C_2) connected across its two ends. These three components are arranged in the shape of the Greek letter π. Circuit diagram is shown in Figure (7.8a) and (7.8 b).

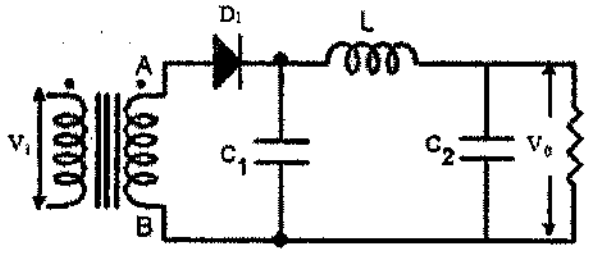


Fig. 7.8 (a) Half Wave Rectifier with π-Section Filter

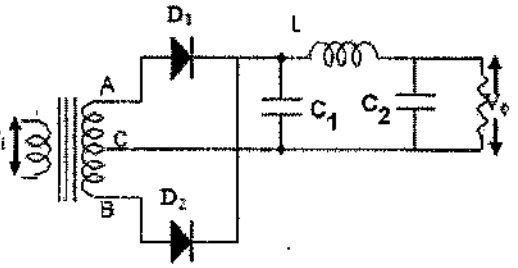


Fig. 7.8 (b) Full Wave Rectifier with π-Section Filter

π Section Filter can be considered as the combination of a shunt capacitor filter containing capacitor C_1 and a L-Section filter containing inductor L and capacitor C_2. When, rectifier output increases the capacitor C_1 charges to the peak value of the rectified output. And when rectifier output decreases the capacitor C_1 discharges through L-Section filter & load R_L and maintain voltage across load very near to the peak value V_m.

7.4 REGULATED POWER SUPPLIES

In an unregulated power supply, the output voltage changes, when input supply voltage or load resistance changes. The aim of voltage regulator circuit is to reduce these variations to zero or at least to some minimum possible value. There are several types of voltage regulators. Among them a few are as follows:

(i) Zener Diode Shunt Regulator
(ii) Transistor shunt Regulator
(iii) Transistor series Regulator

7.4.1 Zener Diode Shunt Regulator

Circuit diagram of a Zener diode shunt regulator is shown in Figure (7.9).

Figure (7.9) consists of a resistor R connected in series with the input voltage, and a Zener diode connected in parallel with load R_L. The input voltage V_{in} is the unregulated output of the rectifier. Let V_Z be the breakdown voltage of Zener diode and I be the current through resistance R. Then out put voltage across R_L will be equal to V_Z. Thus

$$V_Z = V_{in} - RI$$

And current through Zener diode will be

$$I_Z = I - I_L$$

where I_L is the current through load

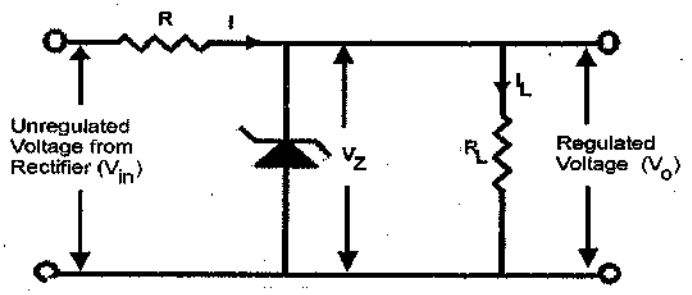


Fig. 7.9 Zener Diode Shunt Regulator

When load current I_L increases (because of the reduction in load resistance), then Zener current I_Z falls in same amount and voltage across resistance R remains constant. Hence output voltage remains constant. When Load current I_L decreases, then Zener diode passes extra current and keeps current I constant.

When input voltage V_{in} increases, then Zener diode passes extra current so that voltage is dropped across R. If input voltage V_{in} decreases then Zener current also decreases and voltage drop across R is reduced. Zener diode maintains constant voltage across load resistance by self adjusting mechanism of adjusting voltage drop across R.

7.4.2 Transistor Shunt Regulator

Circuit diagram of transistor shunt regulator is shown in Figure (7.10).

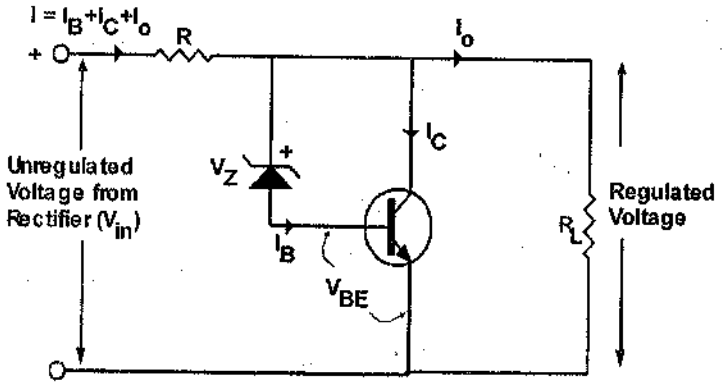


Fig. 7.10 Transistor Shunt Regulator

From Figure (7.10) we can observe that the path AB is parallel to voltage V_0 across load R_L. Thus, from Kirchoff's voltage Law –

$$V_0 - V_Z - V_{BE} = 0$$

or $$V_{BE} = V_0 - V_Z$$

and $$V_i = V_R + V_0$$

or $$V_0 = V_i - V_R$$

We know that Zener voltage V_Z is fixed. Any change in V_0 will cause change in V_{BE} in same direction i.e. if V_0 increase then V_{BE} will also increase and vice-versa. When Base emitter voltage (V_{BE}) decreases then base current (I_B) also decreases. As a result, collector current $I_C (=\beta I_B)$ decreases.

The current (I) through resistance R is –

$$I = I_B + I_C + I_0$$

Thus, due to decrease in output voltage there will be decrease in current (I) and hence decrease in voltage (V_R) across resistance R. Consequently, $V_0 (= V_i - V_R)$ increases.

7.4.3 Transistor Series Regulator

Circuit diagram of transistor series regulator is shown in Figure (7.11) in which transistor is connected in series with load resistance R_L.

The above circuit is also known as emitter follower. In this circuit, transistor acts like a variable resistance whose value is decided by the base current. The Zener voltage V_z is equal to the sum of load voltage V_0 and base-emitter voltage V_{BE}. *i.e.*

$$V_Z = V_0 + V_{BE}$$

$$V_{BE} = V_Z - V_0$$

When load current increases due to decrease in load resistance R_L then V_0 decreases. We know that Zener voltage V_Z is fixed. Thus decrease in V_0 causes increase in V_{BE}. This leads to decrease in collector-emitter resistance of the transistor which will increase the input current and maintain constant voltage V_0 across load R_L.

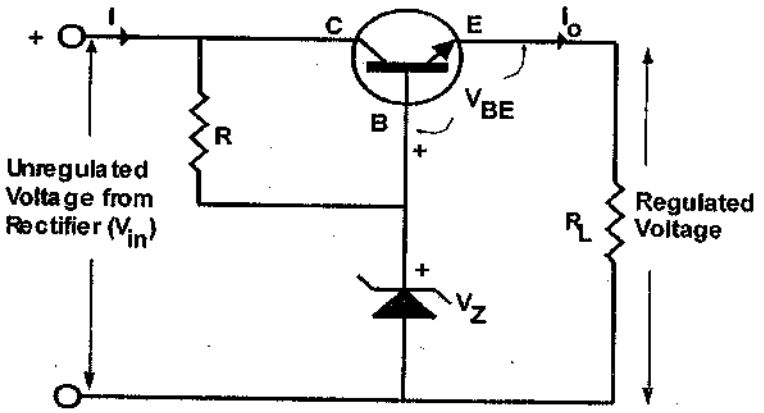


Fig. 7.11 Transistor Series Regulator

7.5 SWITCH MODE POWER SUPPLY (SMPS)

A typical application of a power supply is to convert AC voltage into regulated DC voltages required for electronic equipments. Nowadays, in most of the power supplies the energy flow is controlled with semiconductors, which are continuously switching on and off with high frequency. Such devices are known as switch mode power supply.

SMPS offer greater efficiency in comparison to the Linear Power Supplies (LPS), because a switch can control energy flow with low losses. When a switch is on, it has low voltage drop and pass the current and when switch is off it will block the current. As a result, in such a switch the power dissipation in both states will be relatively low. Due to reduced size of components and lower heat generation, the size and weight of the SMPS is small in comparison to LPS.

Block diagram of a typical SMPS is shown in Figure (7.12).

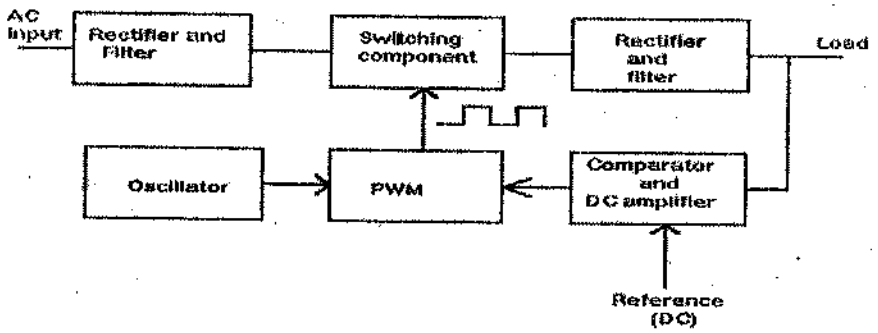


Figure 7.12: Block diagram of SMPS

In SMPS, the AC input is rectified and filtered to give a steady DC voltage. This DC input to the voltage switching block is either blocked or allowed to pass through depending on the state of the switch. The resultant square wave is rectified and filtered. If the current required at the load is high, then the switching control ensures that the voltage switch is on for longer periods.

The sampling is done by a comparator and DC amplifier along with a DC reference. The output voltage is compared with a DC reference. If the output voltage reduces due to increase in load current, the comparator sends a positive signal to the pulse width modulator and increase the on time of the pulse.

Advantages of SMPS

- The Switching devices of the Switching Regulators do not conduct all the time. This in creases the efficiency of the regulators. The SMPS has an efficiency ranging from 50 to 90 percent compared to normal efficiency of a linear regulator which is around 50 percent.
- To regulate the output voltage the switching regulators usually use on off duty cycle of a tran sistor switch. By choosing higher duty cycle frequency, the transformers, and other filter ele ments such as capacitors and inductors can be made very light and expensive

- SMPS can be designed to incorporate inbuilt step up, step down and electrical isolation.

Disadvantages of SMPS

- Due to high switching current, the Switching regulators generate electromagnetic and radio frequency interference noise. This noise can interfere with the equipment such as television, radio and telephones.
- SMPS is costly and more complex than linear regulators.

7.6 SUMMARY

- A piece of equipment which converts alternating voltage/current to direct voltage/current. Such devices are known as Rectifier. The process of conversion of AC voltage/current to DC voltage/ current is known as Rectification
- The circuits/devices which remove the ac component from the pulsating voltage are known as smoothing Filter.
- The circuits/device, which removes the dependence of output voltage on load, is known as Regulators.
- Rectifiers are two types, (i) Half Wave Rectifier, which conducts during one half of the applied AC voltage and, (ii) Full Wave Rectifier, which conducts for full wave of the applied AC voltage.
- Remaining pulsation in output voltage or current is known as Ripple. Ripple factor of Half wave rectifier is 121%.
- Maximum efficiency of half wave rectifier is 40.6 %.
- Ripple factor of Full wave rectifier is 48.2%.
- Maximum efficiency of half wave rectifier is 81.2 %.
- There are many types of filter. Among them, a few important filters are as follows-

(i) Shunt Capacitor Filter
(ii) Series Inductor Filter
(iii) L-Section Filter
(iv) π–Section filter

- Shunt capacitor filter is the cheapest and simplest filter. A capacitor C of large value is connected in shunt with the load resistance R_L.
- In series inductor filter an inductor coil of high inductance is connected in series with the load R_L.
- In L-section filter an inductor L is connected in series and Capacitor C in shunt with load R_L.
- In π–Section Filter consists of one inductor (L) and two capacitors (C_1 and C_2) connected across its two ends.
- The aim of voltage regulator circuit is to reduce the variations in output voltage due to change in input supply voltage or change in load resistance.
- SMPS offer greater efficiency in comparison to the Linear Power Supplies (LPS), because a switch can control energy flow with low losses

7.7 REVIEW QUESTION

Q.1. What do you mean by Rectification? Draw the circuit diagram of a half wave rectifier and explain its operation. Draw the input an output waveform of the half wave rectifier.

Q.2. Drive expression for (i) Average pulsating current (ii) RMS value of pulsating current (iii) Effi ciency (iv) Ripple factor and (v) voltage regulation of a half wave rectifier.

Q.3. Draw the Circuit diagram of full wave rectifier using two PN-junction diode. Draw the input an output waveform and explain its operation.

Q.4. Prove that the efficiency and ripple factor of a full wave rectifier is 81.2% and 48.2 % respec tively.

Q.5. Draw the circuit diagram of full wave rectifier with shunt capacitor filter. Explain its operation and draw the input and output wave form.

Q.6. What do you mean by filters? Draw the circuit diagram of a full wave rectifier with series

inductor filter and explain its operation.

Q.7. Write short note on-

(i) L–Section filter

(ii) π–Section filter

Q.8. What do you mean by voltage regulation? Explain the use of Zener diode as voltage regulator.

Q.9. Draw the circuit diagram of a transistor shunt regulator and transistor series regulator and explain how the voltage stabilization is achieved in these circuits.

Q.10. Draw the Block diagram of a switch mode power supply and explain its advantage and disad vantage.

Unit-08
TRANSISTORS

Content of the Unit

8.1 OBJECTIVE

In this chapter we will discuss –

- Bipolar Junction Transistor and Type of Transistor
- Transistor biasing
- Basic Principle of operation of Transistor
- Different Configurations of Transistor
- Input and output characteristic curves of transistor in different configuration
- Hybrid (h-parameters) of transistor
- Hybrid parameters and equivalent circuit diagram in different configuration of transistor

8.2 INTRODUCTION

The bipolar transistor was invented in 1945 by Shockley, Brattain, and Bardeen at Bell Laboratories. Later on in 1956 they are awarded Nobel Prize. The invention of transistor completely revolutionized the electronic industry. Since then, transistor has led to all kinds of related inventions like Integrated circuits, Optoelectronics devices and Microprocessors. Now-a-days, almost all electronic equipment are designed using semiconductor devices.

The advantages of three terminal solid state devices (Transistor) over the vacuum tubes are as follows–

- They are smaller and light weight.
- There is no heater requirement; hence no heating losses and heating delay.
- They requires very low operating voltages
- They had rugged construction; hence they are shock proof.
- They absorb less power thus they are more.

Transistor is a contraction of two words transfer and resistor. Because, a transistor basically a resistor which amplifies electrical signals as they are transferred through it from its input to output terminals. The junction transistor is also known as bipolar junction transistor because in this device the conduction takes place by the motion of both polarities i.e. electron and holes.

8.3 BIPOLAR JUNCTION TRANSISTORS

The transistor is a three layer semiconductor device consists of three doped regions forming a sandwich. The middle region is called *base* and the two outer regions are called *emitter* and *collector* respectively. Transistor consists of either two *n*-type and one *p*-type layers of material or two p-type and one n-type layers of material. Former is called an NPN transistor and later is called PNP transistor. NPN and PNP transistors along with their circuit symbols are shown in Figure 8.1 (a) &(b) and Figure 8.1 (c) & (d) respectively

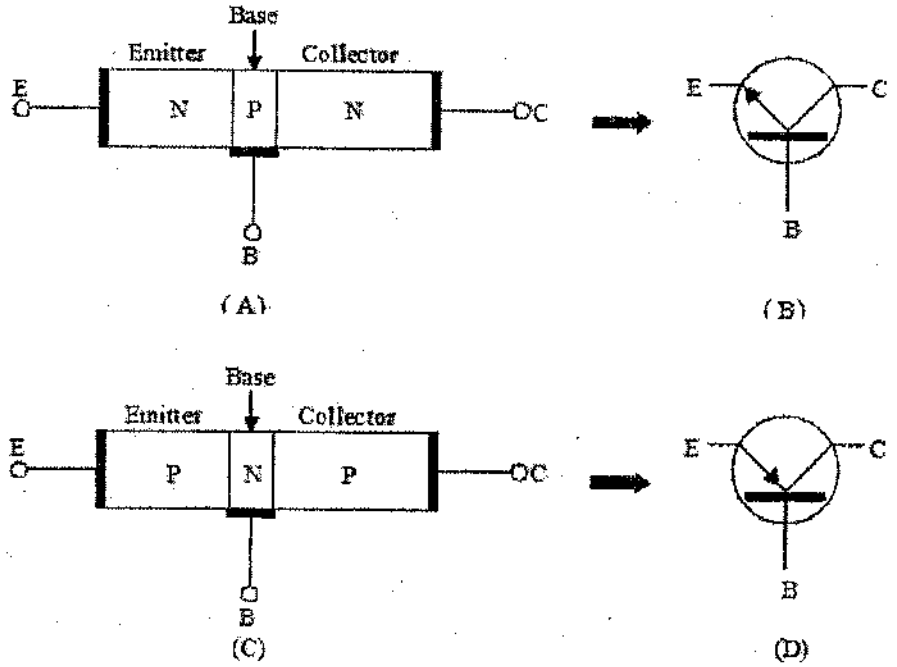


Figure 8.1: (A) NPN Transistor (B) NPN Transistor symbol.
(C) PNP Transistor (D) PNP Transistor symbol.

The emitter, base and collector are provided with terminals which are labeled as E, B and C. The junction between Emitter and base is known as *emitter base junction* (J_{EB}) and junction between Base and collector is known as *collector base junction* (J_{CB}). The emitter is heavily doped because it acts as the source of charge carriers. The base region is very lightly doped and very thin (10^{-6}m). In most of the transistor, the collector region is kept physically largest because it has to dissipate more heat in comparison to emitter region. The doping concentration of collector region is in between that of the emitter and base region. The main function of this region is to collect majority charge carriers coming through the base.

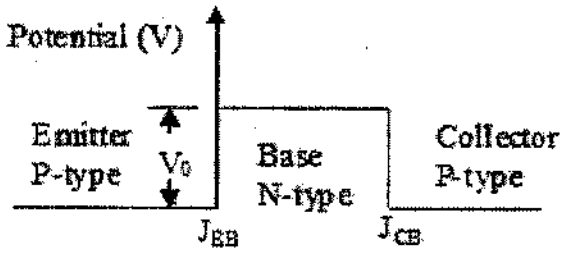
Arrow sign in the symbol diagram of NPN and PNP transistor indicates–

(i) Position of Emitter (E) (ii) Type of Transistor (iii) Direction of Current

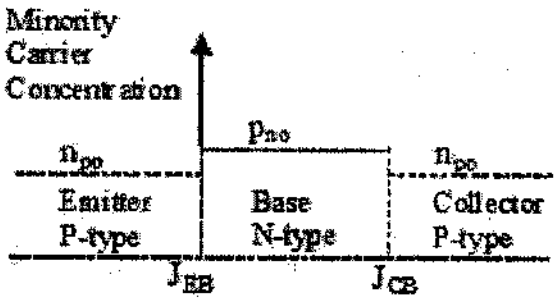
In NPN transistors electrons are the majority charge carriers which moves from emitter E to base B, i.e. direction of conventional current is from base B to emitter E. Similarly, holes are the majority charge carrier in PNP transistor and they moves from emitter E to base B. Thus the direction of conventional current in PNP transistors is from emitter E to base B.

8.4 OPEN CIRCUIT TRANSISTOR

When no external biasing voltages are applied across the transistor then all transistor currents must be zero i.e. there is no free charge carriers crossing each junction. This is possible only if, the potential barrier at junctions adjust themselves to the contact difference of the potential V_0.For the sake of simplicity; let us consider an PNP transistor which has completely symmetrical junction, i.e. emitter and collector regions has similar size and doping concentration. Thus the barrier height will be equal at the emitter base junction J_{EB} and at collector base junction J_{CB}, as shown in Figure (8.2a).



(a) Potential barrier at junctions in each section of an open circuited sysmmetrical PNP transistor.



(b) Minority carrier density in each sectino of an open circuited sysmmetrical PNP transistor.

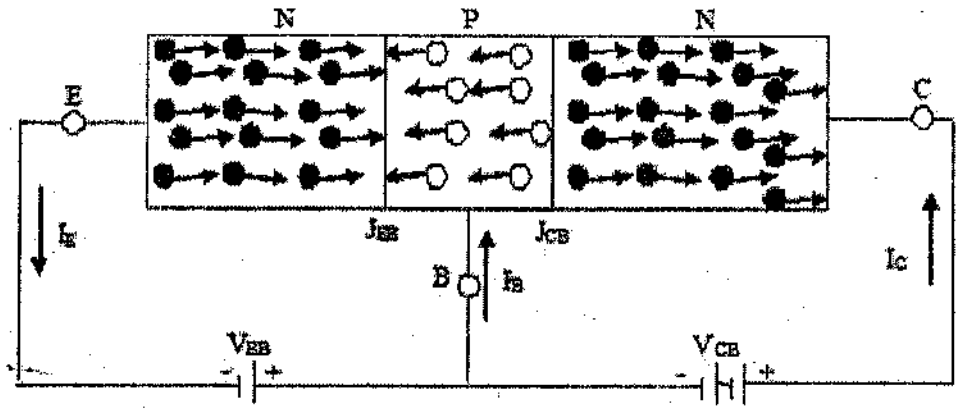
Figure 8.2:

In open circuited condition the minority charge carrier concentration is constant in each region and is equal to its thermal equilibrium value. Thus P-type emitter and collector has minority charge carrier concentration as n_{po} and N-type base has minority charge carrier concentration as p_{no} as shown in Figure (8.2 b).

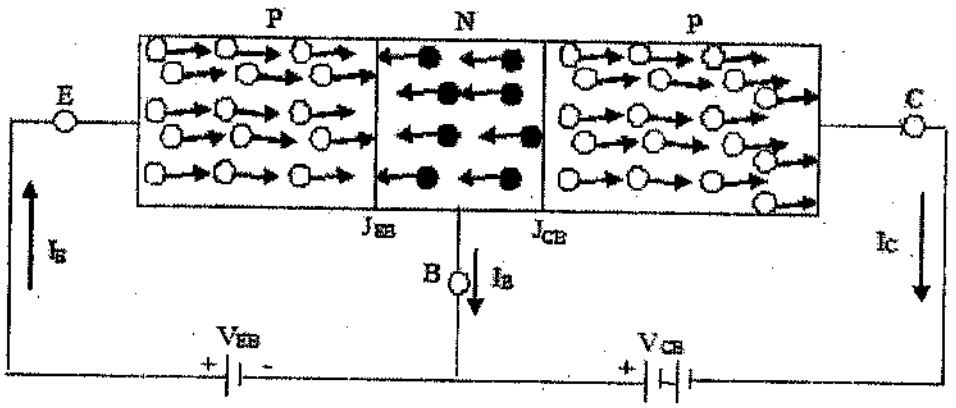
Thus, a PNP transistor can be considered as combination of two back-to-back connected PN junctions. Hence the theory developed for PN junction can be used for explaining the behavior of a transistor.

8.5 TRANSISTOR BIASING IN THE ACTIVE REGION

For the active operation of transistor, voltage bias is applied in such a way so that emitter base junction (J_{EB}) should always be forward biased ($V_{BE} > 0$) and collector base junction (J_{CB}) should always be reversed biased ($V_{BC} < 0$). Under these conditions, device is said to be biased in the "forward active region" or simply in the "active mode." Biasing condition of NPN and PNP transistors are shown in Figure (8.3 a) and (8.3 b).



(a) Biasing of NPN Transistor.



(b) Biasing of PNP Transistor.

Figure: 8.3

8.6 BASIC PRINCIPLE OF OPERATION

As shown in Figure 8.3 (b), for the active operation of PNP the P-type of emitter is kept at positive potential while P-type collector is kept at negative potential. The forward bias across J_{EB} junction of PNP transistor lowers the barrier potential (or reduces the width of the depletion layer) by $|V_{EB}|$ and reverse bias across J_{CB} junction increases the barrier potential by $|V_{CB}|$. So majority charge carrier hole of P-Type (emitter) are repelled by the positive terminal of the battery and injected into N-Type (Base) by crossing the junction. Simultaneously, Minority charge carrier electron of N-Type (Base) are attracted by the positive terminal of the battery and they injected into P-Type (Emitter) by crossing the junction. Resultant emitter current (I_E) is due to flow of charge carriers is sum of current (I_{pE}) due to majority charge carrier holes moving from P-type emitter to N-type base and current (I_{eB}) due to minority charge carrier electrons moving from N-type base to P-type emitter.

But, the number of majority charge carrier hole of P-type emitter is large in comparison to the number of minority charge carriers electron of N-type base and also, during injection process from base to emitter most of the minority charge carrier electrons of P-type base recombine with the majority charge carrier holes of N-type emitter. Thus in PNP transistor emitter current (I_E) is essentially due to majority charge carriers holes of the P-type emitter.

As thickness of the base is kept very small, so most of the injected holes from emitter to base cross the base region without recombination and injected into the P-type collector region. In collector region they are attracted by the negative terminal of the battery. In PNP transistors, the collector current (I_C) is due to injected holes.

In a PNP transistor the number of holes crossing J_{EB} junction is more than the number of holes crossing J_{CB} junction. Base current (I_B) is equal to the difference of the emitter current (I_E) and collector current (I_C).

Collector current (I_C) is less than the emitter current (I_E) due to following reasons –

(i) Emitter current is due to the flow of majority charge carriers holes of P-type emitter and minority charge carrier electrons of N-type base, while collector current (I_C) is only due to majority charge carrier holes of P-type emitter injected into the P-type collector region.

(ii) Some of majority charge carrier holes of P-type emitter recombine in N-type base region.

Active operation of NPN transistor can also be understood with the help of above mentioned description.

8.7 CURRENT COMPONENTS IN A TRANSISTOR

As we discussed in section 8.5, the emitter current (I_E) is sum of current due to the majority charge carriers of emitter and minority charge carriers of base i.e.

For NPN transistor –

$$I_E(e) = I_{eE} + I_{pB}$$

For PNP transistor –

$$I_E(p) = I_{pE} + I_{eB}$$

But current due to minority charge carriers (I_{pB} or I_{eB}) is negligibly small. Thus the emitter current For NPN transistor–

$$I_E(e) \approx I_{eE}$$

For PNP transistor–

$$I_E(p) \approx I_{pE}$$

Collector current is combination of current due to majority carriers and current due to minority carriers, i.e.

$$I_C = (I_C)_{majority} + (I_{CO})_{minority}$$

Fraction of collector current due to minority carriers is known as *leakage current* (I_{CO}). Symbol I_{CO} represent the collector current when emitter terminal is open.

8.8 CHARACTERISTIC CURVES

There are three types of circuit connections (called configuration) for operating a transistor.

(i) Common Base (CB) configuration

(ii) Common Emitter (CE) configuration

(iii) Common Collector (CC) configuration

Here term *common* is used to denote the electrode which is common to input and output circuits.

8.8.1 Common Base (CB) Configuration

Figure (8.4 a) and (8.4 b) shows the common base configuration of PNP and NPN transistor respectively. In this configuration the Base terminal of the transistor is common to input and output.

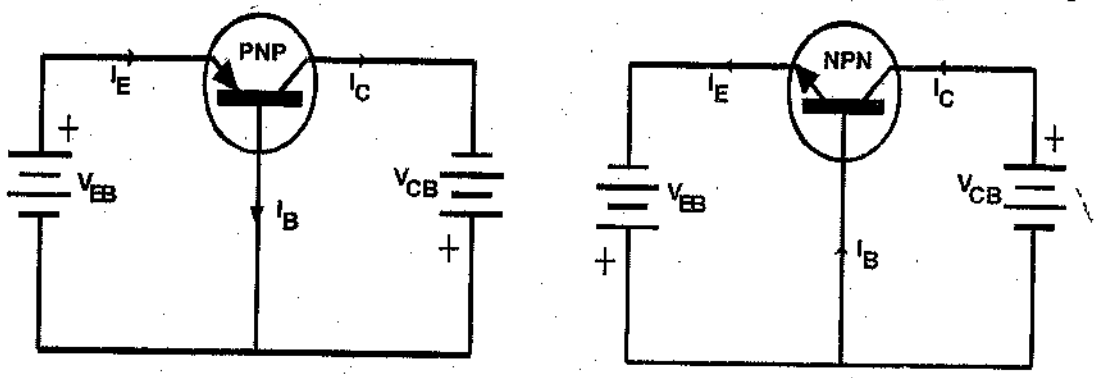


Figure 8.4 (A) Biasing of PNP Transistor in Common Base Configuration
(B) Biasing of NPN Transistor in Common Base Configuration

8.8.1.1 Input Characteristic Curve

The input characteristic curve of CB configuration shows the variation of emitter current I_E with the emitter base voltage V_{EB} while Collector Base voltage V_{CB} is constant. The input characteristic curve of CB-Configuration is shown in the Figure (8.5).

Following conclusion can be drawn from the input characteristic curve of CB-Configuration –

(i) When emitter voltage V_{EB} is increased, the emitter current I_E is very small for a certain value of V_{EB} and this minimum value of V_{EB} does not change with the change in collector base voltage V_{CB}. For Germanium transistor minimum value of V_{EB} is 0.1 volt and for Silicon transistor it is 0.5 Volts.

(ii) For a constant value of V_{CB}, when emitter voltage V_{EB} is increased further, the emitter current I_E increases.

(iii) When V_{CB} is increased, then same emitter cur-

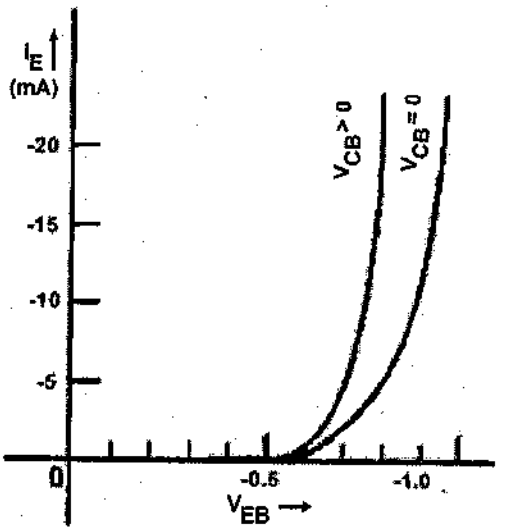


Figure 8.5 Input Characteristic Curve of Transistor in CB Configuration

rent I_E flow for higher value of emitter base voltage V_{EB}.

The Input characteristic curves may be used to find the dynamic input resistance of the transistor and given by-

$$r_i = \left(\frac{\Delta V_{EB}}{\Delta I_E}\right)_{V_{CB}\ Constant}$$

8.8.1.2 Output Characteristic Curve

Output characteristic curve shows the variation of collector current I_C with the change in collector base voltage V_{CB} at constant emitter current I_E. Output characteristic curve are shown in Figure (8.6).

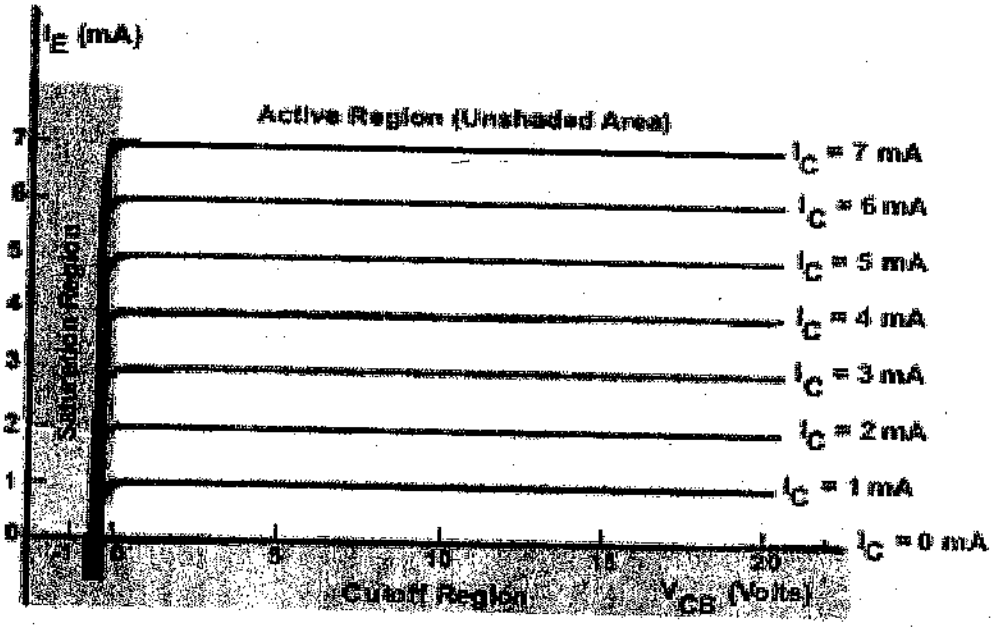


Figure 8.6 Output Characteristic Curve of Tmaistor in CB configuration

Output characteristic curves may be divided in three regions of operation

(a) Active Region (b) Saturation Region (c) Cut-off region

(a) **Active Region:** In this region emitter base junction J_{EB} is forward biased and collector base junction J_{CB} is reversed bias. When emitter current I_E=0 then collector current I_C is equal to the reverse saturation voltage I_{CO}. For non-zero emitter current I_E the collector current I_C is independent of collector base voltage V_{CB} and primarily depends upon emitter current I_E. The relation between I_E and I_C is as follows:

$$I_E \approx I_C$$

(b) Saturation Region: In this region both J_{EB} and J_{CB} junctions are forward biased. This region is towards to left of ordinates V_{CB}=0 and I_E=0. In saturation region collector current I_C changes rapidly with the small change in collector base voltage V_{CB}.

(c) Cutoff Region: In cutoff region both J_{EB} and J_{CB} junctions are reverse biased. This condition exist in the region below and right to the I_E=0 of the characteristic curves

The dynamic output resistance of the transistor is given by-

$$r_o = \left(\frac{\Delta V_{CB}}{\Delta I_C}\right)_{I_E\ Constant}$$

The ratio of collector current and emitter current is known as D.C. current amplification factor $\acute{a}_{dc}$.

$$\alpha_{dc} = \frac{I_C}{I_E}$$

In dynamic state, ratio of change in output collector current ΔI_C to change in input emitter current ΔI_E is known as A.C. current amplification factor α_{ac} -

$$\alpha_{ac} = \frac{\Delta I_C}{\Delta I_E}$$

8.8.2 Common Emitter (CE) Configuration

Common emitter configuration of PNP and NPN transistor is shown in Figure (8.7 a) and (8.7 b). In this configuration Emitter terminal of the transistor is common to Input and Output.

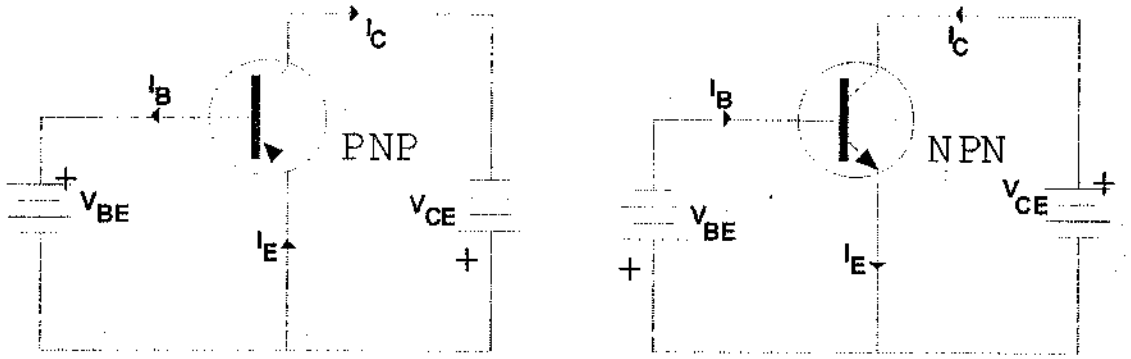


Figure 8.7 (A) Biasing of PNP Transistor in Common Emitter Configuration
(B) Biasing of NPN Transistor in Common Emitter Configuration

8.8.2.1 Input Characteristic Curve

These characteristic curve shows the variation of base current I_B with the change in base emitter voltage V_{BE} when collector emitter voltage V_{CE} is held constant at a particular value. Input characteristic curve of CE-configuration are shown in Figure (8.8). From these curves we can draw following conclusions:

(i) Input characteristic curve of CE configuration is similar to forward biased PN-junction diode. i.e. input base current (I_B) increases with the increase in base-emitter voltage (V_{BE}).

(ii) For constant base-emitter voltage V_{BE}, base current (I_B) decreases with the increase in collector emitter voltage (V_{CE}).

The Input characteristic curves may be used to find the dynamic input resistance of the transistor and given by-

$$r_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE}\ Constant}$$

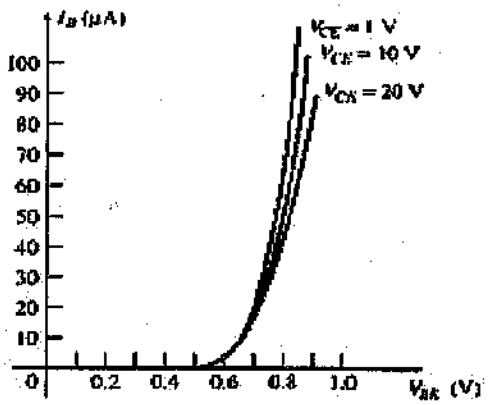


Fig. 8.8 Input Characteristics Curve of Common Emitter Configuration

8.8.2.2 Output Characteristic Curve

Curve between Output collector current (I_C) and collector emitter voltage (V_{CE}) at constant Input base Current (I_B) are known as output characteristic curve of CE-Configuration of transistor. Output characteristic curve are shown in Figure (8.9). Output characteristic curves may be divided in three regions of operation

(a) Active Region
(b) Saturation Region
(c) Cut-off region

(a) Active Region: In this region emitter base junction J_{EB} is forward biased and collector base junction J_{CB} is reversed bias. In this region, V_{CE} is of the order of tens of volts and base current $I_B > 0$.

I_B curves in active region are not completely parallel to the axis.

(b) Saturation Region: In this region both J_{EB} and J_{CB} junctions are forward biased. This region is towards to left of ordinates V_{CE}=0 and I_C=0. In saturation region collector current I_C changes rapidly with the small change in collector base voltage V_{CB}.

(c) Cutoff Region: In cutoff region both J_{EB} and J_{CB} junctions are reverse biased. This condition exist in the region below and right to the I_B=0 of the characteristic curves.

The dynamic output resistance of the transistor is given by-

$$r_o = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B\ Constant}$$

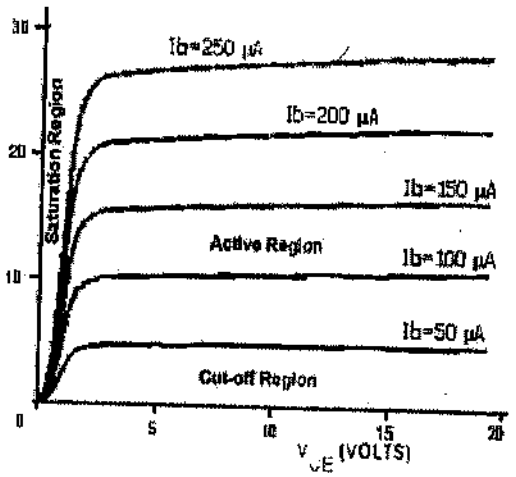


Fig. 8.9 Output Characteristics Curve of Common Emitter Configuration

The ratio of collector current and base current is known as D.C. current amplification factor α_{dc}.

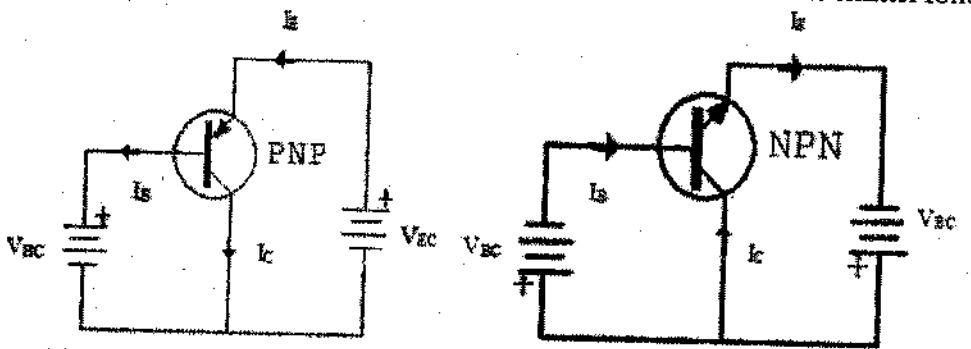
$$\beta_{dc} = \frac{I_C}{I_B}$$

In dynamic state, ratio of change in output collector current ΔI_C to change in input Base current ΔI_B is known as A.C. current amplification factor β_{ac}.

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}$$

8.8.3 Common Collector (CC) Configuration

Common Collector configuration of PNP and NPN transistor is shown in Figure (8.10 a) and (8.10 b). In this configuration collector terminal of the transistor is common to Input and Output. CC-configuration of the transistor is used for impedance matching, because in this configuration Input impedance is high and output impedance is low. This is also known as emitter follower circuit.



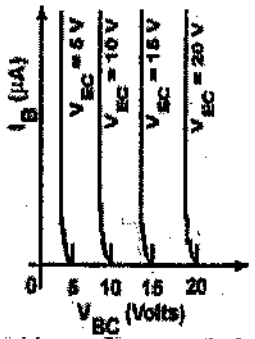
(a) Biasing of PNP transistor in common collector configuration

(b) Biasing of NPN transistor in common collector configuration.

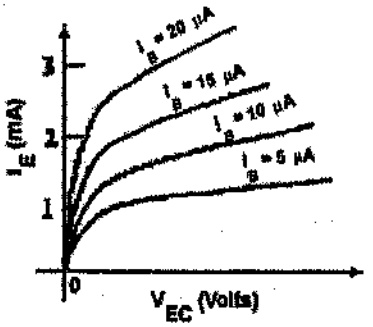
Figure: 8.10

The Common collector configuration is a special case of the common emitter configuration. In CC-Configuration the output characteristics curves are drawn between I_E and V_{EC} which are similar to the output characteristic curves of common emitter configuration between I_C and V_{CE} because $I_E \cong I_C$ and $|V_{EC}| = |V_{CE}|$.

The characteristic curves of CC configurations are shown in Figure (8.11 a) and (8.11 b).



(a) Input characteristic curve for collector configuration



(b) Output chractersitics curve of common collector configuation.

Figure: 8.11

8.8.4 Current Relations

We know that for a junction transistor-

$$I_E = I_B + I_C$$

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$$

$$\frac{1}{\alpha_{dc}} = \frac{1}{\beta_{dc}} + 1 = \frac{1+\beta_{dc}}{\beta_{dc}}$$

$$\alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}}$$

or $$\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}}$$

8.9 EXPRESSIONS FOR HYBRID PARAMETERS OF A TRANSISTOR

In general, four terminal networks, as shown in Figure (8.12) may be studied without detailed knowledge of internal circuitry of the network in terms of some parameters used in measurement of voltages and current at the output and input terminals. If I_1 and V_1 be the input current and Input voltage respectively and I_2 and V_2 be the output current and output voltage respectively. Then two variables may be chosen arbitrarily as impendent variables leading two equations which can be solved for other two variables.

In the entire three configurations (CB, CE & CC), transistor may be regarded as four terminal network. For example, in CE configuration base and common emitter acts as input terminal while collector and emitter acts as output terminal. In transistor analysis it is useful to choose input current I_1 and output voltage V_2 as independent variable and input voltage V_1 and output current I_2 as independent variables. i.e.

$$V_1 = f(I_1, V_2)$$

$$I_2 = f(I_1, V_2)$$

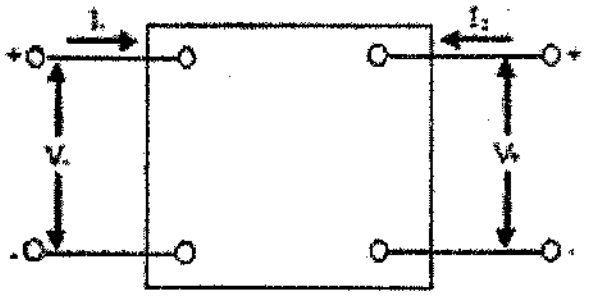


Figure 8.12: Four terminal network.

For small sinusoidal signals limited to the quasi-linear region (Active Region) of transistor these dependence can be written in terms of linear equation as follows–

$$V_1 = h_{11} I_1 + h_{12} V_2$$
$$I_2 = h_{21} I_1 + h_{22} V_2$$

The coefficients h_{11}, h_{12}, h_{21}, h_{22} are known as h-parameter or Hybrid parameters.

$h_{11} = \frac{V_1}{I_1}$ = short circuit input impedance when $V_2 = 0$

$h_{12} = \frac{V_1}{V_2}$ = open circuit reverse voltage gain when $I_1 = 0$

$h_{21} = \frac{I_2}{I_1}$ = Short circuit forward current gain when $V_2 = 0$

$h_{22} = \frac{I_2}{V_2}$ = Open circuit output admittance when $I_1 = 0$

Equivalent circuit of four terminal networks is shown in Figure (8.13).

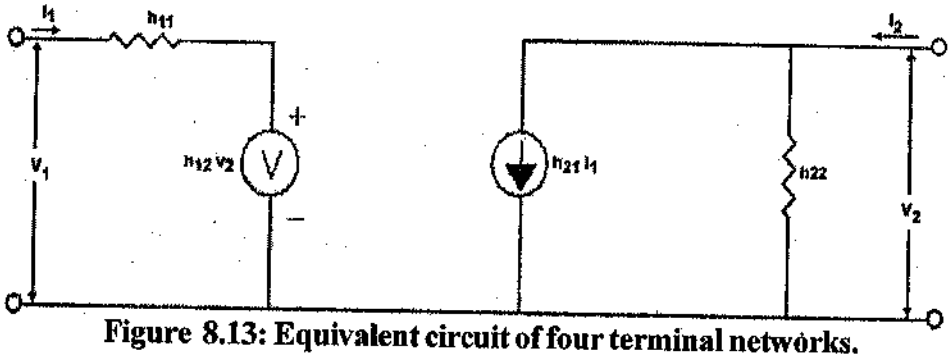


Figure 8.13: Equivalent circuit of four terminal networks.

8.9.1 Hybrid Parameters and Equivalent circuit of CB, CE and CC configuration of the Transistor

(i) Common Base Configuration

Common Base Configuration is shown in Figure (8.14). In this configuration –

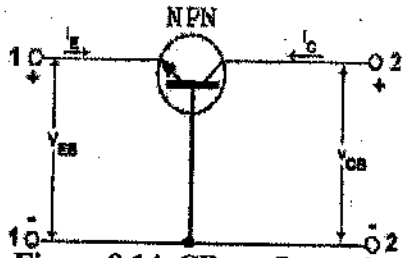


Figure 8.14: CB configuration.

$V_1 = V_{EB}$ $\quad V_2 = V_{CB}$ $\quad I_1 = I_E$ and $I_2 = I_C$

$h_{11} = h_{ib}$ $\quad h_{12} = h_{rb}$ $\quad h_{21} = h_{fb}$ and $h_{22} = h_{ob}$

Thus, hybrid parameter equation for CB configuration of transistor will be

$$V_{EB} = h_{ib} I_E + h_{rb} V_{CB}$$
$$I_C = h_{fb} I_E + h_{ob} V_{CB}$$

If we assume that h-parameters remains constant for signals of small amplitude then -

$$\Delta V_{EB} = h_{ib} \Delta I_E + h_{rb} \Delta V_{CB}$$
$$\Delta I_C = h_{fb} \Delta I_E + h_{ob} \Delta V_{CB}$$

or

$$v_{eb} = h_{ib} i_e + h_{rb} v_{cb}$$
$$i_C = h_{fb} i_e + h_{ob} v_{cb}$$

Input Impedance $(h_{ib}) = \left(\frac{\Delta V_{EB}}{\Delta I_E}\right)_{V_{CB} = \text{Constant}}$

Reverse Voltage Gain $(h_{rb}) = \left(\frac{\Delta V_{EB}}{\Delta V_{CB}}\right)_{I_E = \text{Constant}}$

Forward current Gain $(h_{fb}) = \left(\frac{\Delta I_C}{\Delta I_E}\right)_{V_{CB} = \text{Constant}}$

Output Conductance $(h_{ob}) = \left(\frac{\Delta I_C}{\Delta V_{CB}}\right)_{I_E = \text{Constant}}$

The equivalent circuit of common base configuration is shown in Figure (8.15).

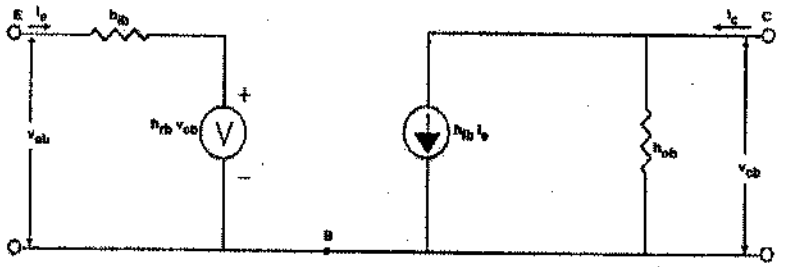


Figure 8.15: h-Parameter equivalent circuit for CB configuratio of transistor.

(ii) Common Emitter Configuration

Common Emitter Configuration is shown in Figure (8.16). In this configuration –

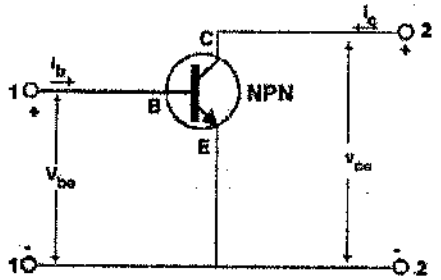


Figure:8.16

$V_1 = V_{BE}$ $V_2 = V_{CE}$ $I_1 = I_B$ and $I_2 = I_C$

$h_{11} = h_{ie}$ $h_{12} = h_{re}$ $h_{21} = h_{fe}$ and $h_{22} = h_{oe}$

Thus, hybrid parameter equation for CB configuration of transistor will be

$$V_{BE} = h_{ie} I_B + h_{re} V_{CE}$$
$$I_C = h_{fe} I_B + h_{oe} V_{CE}$$

If we assume that h-parameters remains constant for signals of small amplitude then -

$$\Delta V_{BE} = h_{ie} \Delta I_B + h_{re} \Delta V_{CE}$$
$$\Delta I_C = h_{fe} \Delta I_B + h_{oe} \Delta V_{CE}$$

or
$$v_{be} = h_{ie} i_b + h_{re} v_{ce}$$
$$i_c = h_{fe} i_b + h_{oe} v_{ce}$$

Input Impedance $(h_{ie}) = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE} = \text{Constant}}$

Reverse Voltage Gain $(h_{re}) = \left(\frac{\Delta V_{BE}}{\Delta V_{CE}}\right)_{I_B = \text{Constant}}$

Forward current Gain $(h_{fe}) = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE} = \text{Constant}}$

Output Conductance $(h_{oe}) = \left(\frac{\Delta I_C}{\Delta V_{CE}}\right)_{I_B = \text{Constant}}$

The equivalent circuit of common base configuration is shown in Figure (8.17).

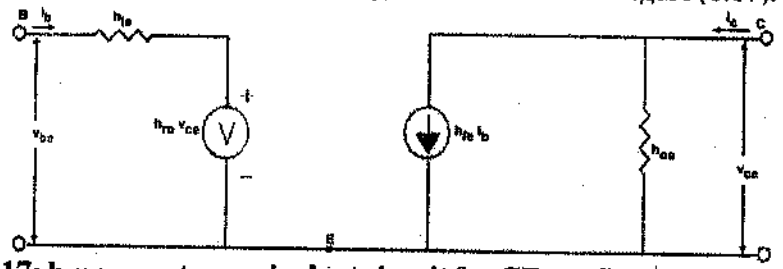


Figure 8.17: h-parameter equivalent circuit for CE configuration of transistor.

(iii) Common Collector Configuration

Common Collector Configuration is shown in Figure (8.18). In this configuration –

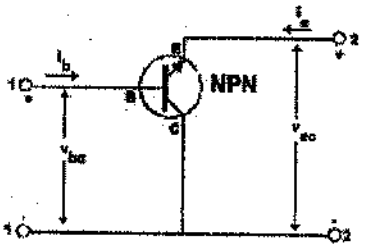


Figure 8.18: CC configuration.

$V_1 = V_{BC}$ $V_2 = V_{EC}$ $I_1 = I_B$ and $I_2 = I_E$

$h_{11} = h_{ic}$ $h_{12} = h_{rc}$ $h_{21} = h_{fc}$ and $h_{22} = h_{oc}$

Thus, hybrid parameter equation for CB configuration of transistor will be

$$V_{BC} = h_{ic} I_B + h_{rc} V_{EC}$$
$$I_E = h_{fc} I_B + h_{oc} V_{EC}$$

If we assume that h-parameters remains constant for signals of small amplitude then -

$$\Delta V_{BC} = h_{ic} \Delta I_B + h_{rc} \Delta V_{EC}$$
$$\Delta I_E = h_{fc} \Delta I_B + h_{oc} \Delta V_{EC}$$

or
$$v_{bc} = h_{ic} i_b + h_{rc} v_{ec}$$
$$i_e = h_{fc} i_b + h_{oc} v_{ec}$$

The equivalent circuit of common base configuration is shown in Figure (8.19).

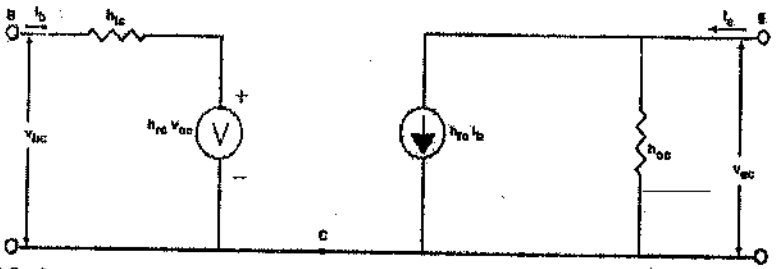


Figure 8.19: h-parameter equivalent circuit for CC configuration of transistor.

8.10 SUMMARY

- The transistor is a three layer semiconductor device consists of three doped regions forming a sand wich. The middle region is called *base* and the two outer regions are called *emitter* and *collector* respectively.
- Transistor consists of either two n-type and one p-type layers of material or two p-type and one n-type layers of material. Former is called an NPN transistor and later is called PNP transistor.
- The junction between Emitter and base is known as *emitter base junction* (J_{EB}) and junction between Base and collector is known as *collector base junction* (J_{CB}).
- Arrow sign in the symbol diagram of NPN and PNP transistor indicates

(i) Position of Emitter (E)
(ii) Type of Transistor
(iii) Direction of Current

- For the active operation of transistor, voltage bias is applied in such a way so that emitter base junction (J_{EB}) should always be forward biased ($V_{BE} > 0$) and collector base junction (J_{CB}) should always be reversed biased ($V_{BC} < 0$).
- The emitter current (I_E) is sum of current due to the majority charge carriers of emitter and minority charge carriers of base.
- Collector current is combination of current due to majority carriers and current due to minority carriers.
- Fraction of collector current due to minority carriers is known as *leakage current* (I_{CO}).
- There are three types of circuit connections (called configuration) for operating a transistor.
  (i) Common Base (CB) configuration
  (ii) Common Emitter (CE) configuration
  (iii) Common Collector (CC) configuration
- In Common Base configuration the Base terminal of the transistor is common to input and output.
- Output characteristic curves may be divided in three regions of operation
  (a) Active Region (b) Saturation Region (c) Cut-off region
- In Active region emitter base junction J_{EB} is forward biased and collector base junction J_{CB} is reversed bias.
- In saturation region both J_{EB} and J_{CB} junctions are forward biased.
- In cutoff region both J_{EB} and J_{CB} junctions are reverse biased.
- In the entire three configurations (CB, CE & CC), transistor may be regarded as four terminal network.

8.11 REVIEW QUESTION

Q.1. What do you mean by bipolar junction transistor? Give the circuit symbols of transistor and explain the behavior of an open circuit transistor.

Q.2. Explain the Biasing and Basic principle of operation of a PNP/NPN transistor in the Active Region.

Q.3. Explain the Different Configurations of a Transistor. What do you mean by Characteristic Curves? Draw Input and Output characteristic curves of a NPN/PNP transistor in different configura tion and explain them.

Q.4. What do you mean by hybrid parameters of a transistor? Explain hybrid parameters and draw equivalent circuit of CB, CE and CC configuration of a NPN/PNP transistor.

Q.5. Define Current gain in common base and common emitter configuration of a transistor and derive relation between them.

◉◉◉◉

Unit-09
APPLUCATION OF TRANSISTORS

Content of the Unit

9.1 OBJECTIVE

In previous chapter we have discussed the physics and operation of a bipolar transistor. In this chapter we will discuss –

- Transistor as an amplifier and characteristics of amplifiers
- Concept of feedback and various feedback network
- Oscillators
- Transistor as an switch
- Field effect Transistor and its characteristics curve

9.2 TRANSISTOR AS AN AMPLIFIER

A voltage-controlled current source along with a load resistor can form an amplifier. In general, an amplifier produces an output (voltage or current) that is a magnified version of the input (voltage or current). The basic amplifier circuit as an active four terminal network is shown in fig. 9.1. Block (A) shown in figure could be a CB, CE or CC configuration of the transistor.

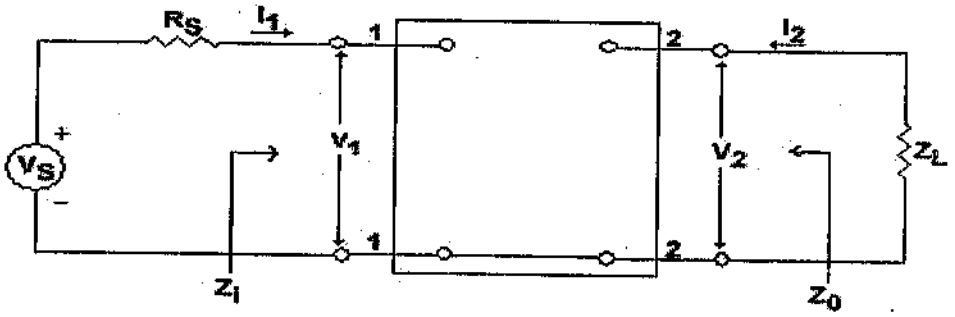


Fig. 9.1 Transistor Amplifier as four terminal Network

The working of a four terminal network is studied using the measured quantities like voltage and current at input and output terminals which are related to each other through h-parameter. Hybrid parameter equations of an amplifier are –

$$v_1 = h_i\, i_1 + h_r\, v_2$$
$$i_2 = h_f\, i_1 + h_o\, v_2$$

where h_i, h_r, h_f and h_o are the hybrid parameters of the transistor. For small alternating or sinusoidal signals h-parameter will be constant within operating limit.

9.3 CHARACTERISTICS OF AN AMPLIFIER

Figure (9.2) and (9.3) are the h-parameter equivalent circuit of transistor amplifier with voltage source and current source respectively.

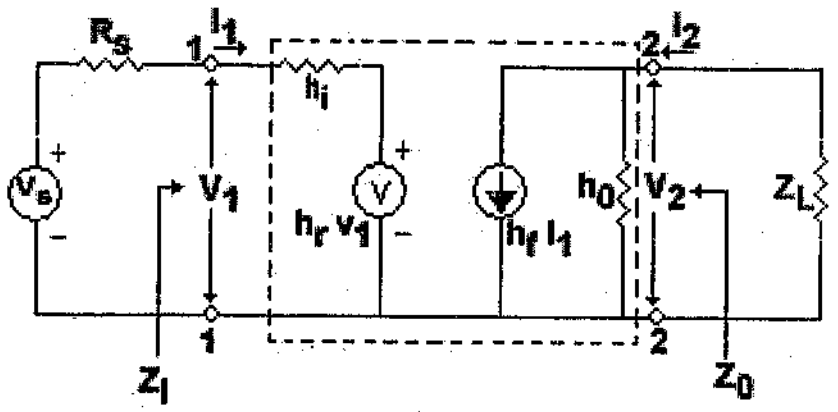


Fig. 9.2: h-parameter equivalent circuit of transistor with input voltage source.

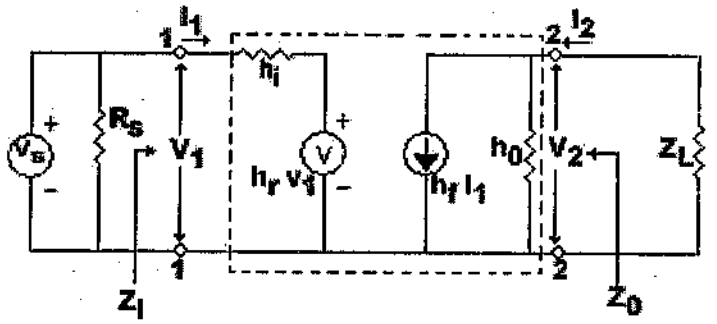


Fig. 9.3 : h-parameter equivalent circuit of transistor with input current source.

(I) Current Gain or Current Amplification (A_i)

The ratio of output current to input current of a transistor amplifier is known as current gain (A_i).*i.e.*

$$A_i = \frac{Output\ Current}{Input\ Current} = \frac{I_2}{I_1}$$

As $v_2 = -i_2 R_L$

$$i_2 = h_f\, i_1 + h_o\,(-i_2 R_L)$$
$$(1 + h_o R_L) i_2 = h_f\, i_1$$
$$A_i = \frac{i_2}{i_1} = \frac{h_f}{(1 + h_o R_L)}$$

(II) Input Impedance (R_i)

Input impedance of a transistor amplifier is the impedance reflected at the input terminal and it is equal to the ratio of input voltage to input current.

$$R_i = \frac{Input\ voltage}{Input\ Current} = \frac{v_1}{i_1}$$

$$= \frac{h_i i_1 + h_r v_2}{i_1}$$

$$= h_i + h_r \left(\frac{-i_2 R_L}{i_1} \right)$$

$$= h_i - h_r R_L \left(\frac{h_f}{(1+h_o R_L)} \right)$$

$$= h_i - \frac{h_r h_f R_L}{(1+h_0 R_L)}$$

(III) Voltage Gain or Voltage Amplification (A_v)

The ratio of output voltage and input voltage is known as voltage gain (A_v) of the transistor amplifier.

$$A_v = \frac{Output\ voltage}{Input\ voltage} = \frac{v_2}{v_1}$$

$$= \frac{(-i_2 R_L)}{v_1} = \frac{(-A_i i_1 R_L)}{v_1}$$

$$= -A_i \frac{R_L}{R_i}$$

$$= -\left(\frac{h_f}{(1+h_o R_L)} \right) \left(\frac{R_L}{h_i - \frac{h_r h_f R_L}{(1+h_0 R_L)}} \right)$$

$$= -\frac{h_f R_L}{h_i + R_L (h_i h_o - h_f h_r)}$$

(IV) Output Impedance (R_0)

Output impedance can be determined by keeping the source voltage V_s at zero voltage and output impedance Z_L is replaced by voltage generator V_2 in Circuit diagram shown in fig. 9.2.If I_2 be the current drawn by the voltage generator V_2 then ratio of Voltage V_2 and current I_2 is called output Impedance Z_0. i.e.

$$\text{Output Impedance} = \frac{V_2}{I_2}$$

From fig. 9.2 h-parameter equations-

$$i_2 = h_f i_1 + h_0\ v_2$$

$$R_s i_1 + h_f i_1 + h_f\ v_2 = v_s = 0$$

$$\therefore\ i_1 = -\frac{h_r\ v_2}{(R_s + h_i)}$$

$$i_2 = \left(-\frac{h_r\ v_2}{(R_s + h_i)}\right) h_f + h_0\ v_2$$

$$i_2 = v_2\left(h_0 - \frac{h_r h_f}{(R_s + h_i)}\right)$$

$$Z_0 = \frac{v_2}{i_2} = \left(h_0 - \frac{h_r h_f}{(R_s + h_i)}\right)^{-1}$$

$$Z_0 = \frac{(R_s + h_i)}{h_0\ R_s + (h_0 h_i - h_f\ h_r)}$$

(V) Power Gain (Ap)

The ratio of output power and input power is known as power gain (A_p) of the transistor amplifier.

$$A_p = \frac{Output\ Power}{Input\ Power} = \frac{v_2}{v_1}\cdot\frac{i_2}{i_1} = |A_V|\cdot|A_i|$$

$$= \left(\frac{h_f}{(1+h_o R_L)}\right)\left(\frac{h_f R_L}{h_i + R_L(h_i h_o - h_f h_r)}\right)$$

$$= \frac{h_f^2\ R_L}{(1+h_0\ R_L)(h_i + R_L(h_i h_o - h_f h_r))}$$

9.4 CONCEPT OF LOAD LINE AND QUIESCENT POINT (Q-POINT)

Circuit diagram of a CE amplifier driven by an input signal voltage V_s of source resistance R_s is shown in Figure (9.4). The Output characteristics of an NPN transistor are shown in Figure (9.5)

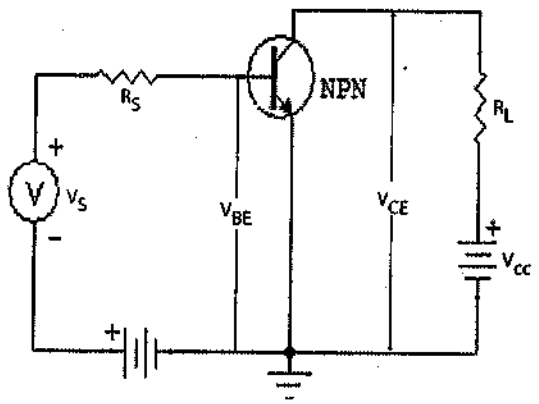


Fig. 9.4 Basic CE Amplifier Circuit

From Kirchhoff's voltage law to the collector circuit of Fig. 9.4, we get-

$$V_{CC} = I_C R_L + V_{CE}$$

When I_C=0 then $V_{CE} = V_{CC}$ (Intercept on Voltage axis)

And when V_{CE} = 0 then $I_C = V_{CC}/R_L$ (intercept on Current axis)

Above equation represent straight line having intercept V_{CC} on the voltage axis and intercept V_{CC}/R_L on the current axis. The Slope of this line is $-1/R_L$. This line is known as the load line and represents the dynamic characteristics of the transistor.

In Figure (9.5) the input bias current I_B is chosen as 60 mA. Now, let us consider that a sinusoidal base current of peak value 20 mA be applied at the input of the CE amplifier. Now base current will varies by ± 20 mA about Quiescent value of 60 mA. For a given instantaneous base current I_B, the point of intersection of collector characteristic curve and the load line gives the corresponding values of I_c and V_{CE}. In our case these values corresponding to point P, A and B are

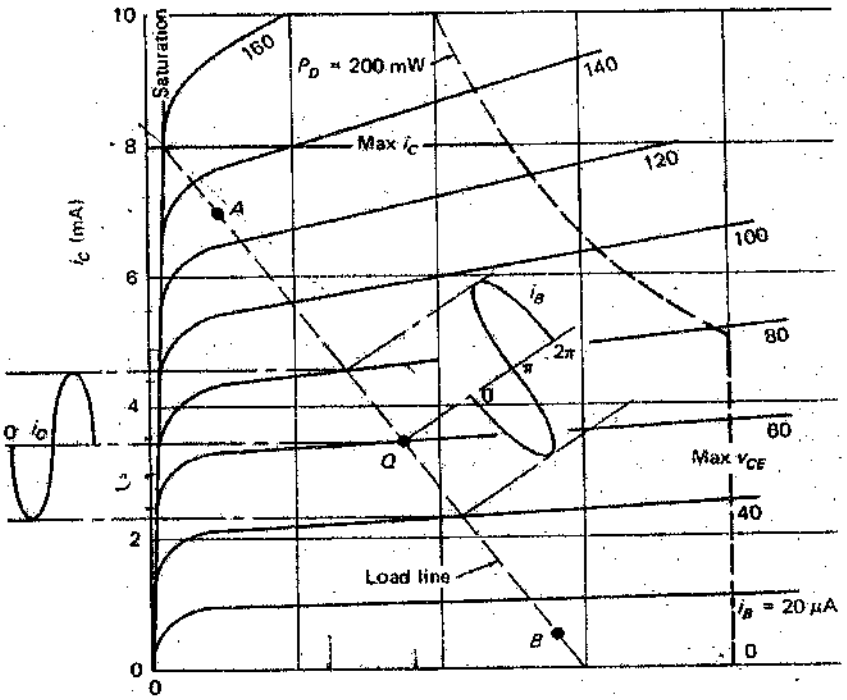


Figure 9.5: Output characteristic curves with Q-point and load line.

Point P	I_B=60 mA,	I_C=3.5mA,	V_{CE}=17.5V
Point A	I_B=80 mA,	I_C=4.5mA,	V_{CE}=13.5V
Point B	I_B= 40 mA,	I_C= 2.3 mA,	V_{CE}= 21.5V

This clearly indicates that if Q point be chosen near E or F on the characteristic curve then it may create signal distortion due to saturation and cut-off. For linear operation, The Q-point must be selected in the central region so that the maximum variable input signal could be applied in the input of the amplifier.

9.5 BIASING IN BJT AMPLIFIER CIRCUIT

Biasing problem of BJT is related to establish constant dc current in the collector of the transistor. The Collector current must be calculable, predictable and it should be insensitive to variations in temperature and to the large variations in the value of b. Another important consideration in biasing design is the selection of the Q-point to allow for maximum output signal swing.

9.5.1 Fixed Bias

Figure (9.6) shows the circuit diagram of fixed bias arrangement which is the most commonly used biasing arrangement of a transistor amplifier. Advantage of this type of biasing arrangement is that in this arrangement of biasing single power supply is used to bias Emitter-Base and Collector base junction. In this circuit constant current is provided at

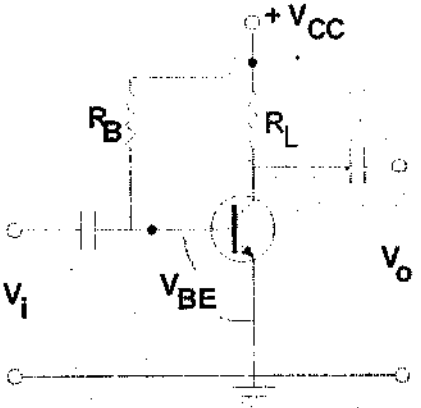


Figure 9.6 Fixed Bias Circuit

the base of transistor with the help of a resistance R_B and voltage source V_{CC}.
From Input loop-

$$V_{CC} - R_B I_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

As V_{BE} (in mV) is small in comparison to the V_{CC} (in Volts) thus we can neglect V_{BE}.

$$\therefore \quad I_B = \frac{V_{CC}}{R_B}$$

Current I_B is constant.
From Output loop-

$$V_{CC} - R_L I_C - V_{CE} = 0$$

$$But \quad I_C = h_{fe} I_B$$

$$\therefore \quad V_{CE} = V_{CC} - h_{fe} R_L I_B$$

In above equation V_{CC} and R_L are constant. Thus due to temperature, if any change occurs in the value of h_{fe} then operating point Q will shift.

9.5.2 Self or Emitter Feed-Back Bias

Self or Emitter feedback bias circuit is shown in Figure (9.7a).In this type of biasing arrangement resistance R_1 and R_2 provides fixed bias and resistance R_E provides stability with the help of negative current feedback. Figure (9.7 b) shows the same circuit with the voltage divider network replaced by Thevenin equivalent-

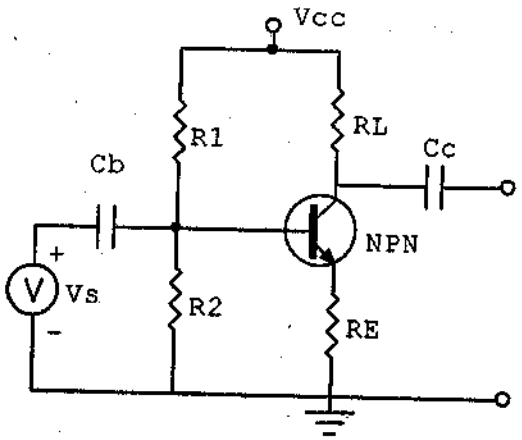


Fig. 9.7 (a) Self or Emitter feedback bias circuit

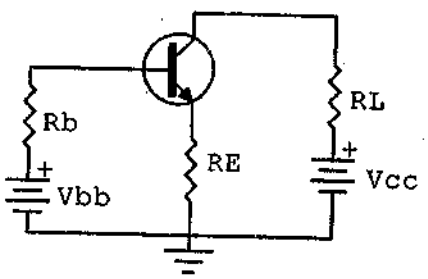


Fig. 9.7 (b) Equivalent Circuit of Self or Emitter feedback bias

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$and \quad R_B = \frac{R_1 R_2}{R_1 + R_2}$$

From Kirchhoff's voltage law to the Collector-emitter circuit of Figure (9.7b)

$$-V_{CC} + I_C (R_L + R_E) + I_B R_E + V_{CE} = 0$$

$$But \; I_B << I_C .Thus \; voltge \; drop \; I_B R_E \; may \; be \; neglected.$$

$$V_{CE} = V_{CC} - I_C (R_L + R_E)$$

From Kirchhoff's voltage law to the base-emitter circuit of Fig. 9.7(b)

$$V_{BB} = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$V_{BB} - V_{BE} = R_B I_B \left(1 + \frac{R_E}{R_B}\right) + I_C R_E$$

$$V_{BB} - V_{BE} = R_B I_B \left(\left(1 + \frac{R_E}{R_B}\right) + \frac{I_C R_E}{R_B I_B}\right)$$

we know that $h_{fe} = \frac{I_C}{I_B}$

$$V_{BB} - V_{BE} = \frac{R_B I_C}{h_{fe}} \left(\left(1 + \frac{R_E}{R_B}\right) + \frac{R_E}{R_B} h_{fe}\right)$$

$$I_C = \frac{V_{BB} - V_{BE}}{R_B} \frac{h_{fe}}{\left(1 + \frac{R_E}{R_B}(1 + h_{fe})\right)}$$

9.6 FEEDBACK

Feedback is a process in which a fraction of output energy is fed back to input. When a fraction of output voltage or output current of an amplifier is fed back to its input then the working efficiency of the amplifier changes. Depending on the phase difference of input signal and feedback signal feedback may be classified in two categories, namely-

(I) Positive feedback or regenerative feedback

When, Input signal and feedback signal are in same phase, then magnitude of input signal increases by addition of feedback signal. This type of feedback is known as positive feedback or regenerative feedback. Positive feedback is used in oscillator circuits.

(II) Negative feedback or degenerative feedback

When, Input signal and feedback signal are in opposite phase then the magnitude of input signal decreases. This type of feedback is known as negative feedback or degenerative feedback. Negative feedback reduces the gain of the amplifier but increases the stability of the amplifier.

9.6.1 Forms of Feedback Circuits

All feedback circuit can be classified in following four categories:

(I) Voltage Series Feedback:

Block diagram of voltage series feedback is shown in Figure (9.8 a).In this type of feedback circuit output terminals of amplifier are connected in parallel with the feedback network. Feed back signal from feedback network is connected in series with the input signal voltage.

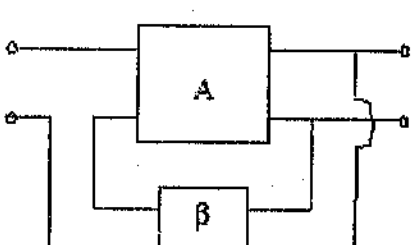


Fig. 9.8 (a) Voltage Series Feedback

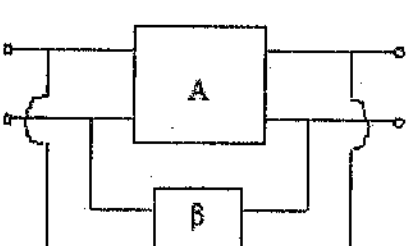


Fig. 9.8 (b) Voltage Shunt Feedback

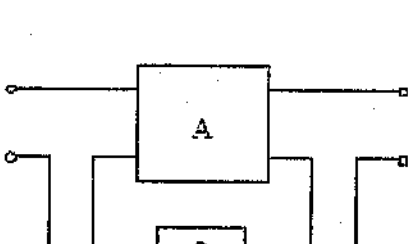


Fig. 9.8 (c) Current Series Feedback

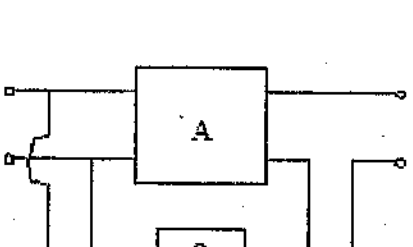


Fig. 9.8 (d) Current Shunt Feedback

(II) · Voltage Shunt Feedback

Block diagram of voltage series feedback is shown in Figure (9.8 b). In voltage shunt feed back circuit output terminals of amplifier are connected in parallel with feedback network. Feed back signal from feedback network is connected in parallel with the input signal voltage.

(III) Current Series Feedback:

Block diagram of voltage series feedback is shown in Figure (9.8 c). In current series feedback circuit output terminals of amplifier are connected in series with the feedback network. Feed back signal from feedback network is connected in series with the input signal voltage.

(IV) Current Shunt Feedback

Block diagram of voltage series feedback is shown in Figure (9.8 d). In current shunt feedback circuit output terminals of amplifier are connected in series with the feedback network. Feed back signal from feedback network is connected in parallel with the input signal voltage.

9.6.2 Principle of Feedback

Block diagram showing the principle of feedback is show in Figure (9.9). In this diagram an amplifier is shown as box. A fraction of amplifier output is fed back to input with the help of a feedback network (shown as another box in the diagram). The network used for feeding signal from output into input is known as â feedback network.

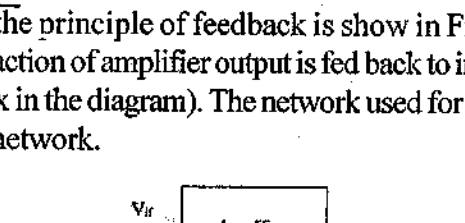


Fig. 9.9 Block Diagram of Principle of feedback

When feedback voltage is fed into the input of the amplifier, the feedback voltage V_f is either added or subtracted from the input voltage.

If resultant voltage at the input of the amplifier is $V_{if} = V_i - V_f$

Then amplifier is said to be negative feedback amplifier and when resultant voltage at the input of amplifier is

$$V_{if} = V_i + V_f$$

Then the amplifier is said to be positive feedback amplifier.

If A be gain of the amplifier without feedback then

$$A = \frac{V_o}{V_i}$$

The gain is often called Open loop gain.

If V_{if} is the input voltage with feedback and V'_o is the output voltage then

$$A = \frac{V'_o}{V_{if}}$$

$$\therefore \quad V_{if} = \frac{V'_o}{A}$$

If â fraction of output voltage V'_o is fed into the output voltage then -

$$V_f = \beta V'_o$$

$$V_{if} = V_i + \beta V'_o$$

$$\frac{V'_o}{A} = V_{if} = V_i + \beta V'_o$$

$$V'_o = \frac{AV_i}{(1 - A\beta)}$$

$$A_f = \frac{V'_o}{V_i} = \frac{A}{(1 - A\beta)}$$

This equation is known as general feedback equation.

In feedback circuit A and â may be positive or negative, real or complex. Therefore-

(I) If $|1 - A\hat{a}| > 1$ i.e. Aâ is negative, then $|A_f| < |A|$. This type of feedback is called negative feedback.

(II) If $|1 - A\hat{a}| = 0$ i.e. Aâ=1 then $|A_f| =$ ".

(III) If $|1 - A\hat{a}| < 1$ i.e. Aâ is Positive, then $|A_f| > |A|$. This type of feedback is called positive feedback.

9.7 OSCILLATORS

Oscillators are self excited active circuits because no external signal is applied at the input of oscillators. In oscillators dc current energy is converted into periodically varying current. Hence the oscillator may be defined as a circuit which generates an A.C. output signal without externally applied input signal or it is a circuit which converts DC energy into AC energy at very high frequency.

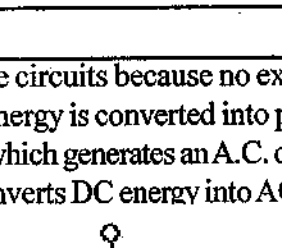


Fig. 9.10 Tank Circuit

Simplest example of a oscillator is a Tank Circuit (Figure 9.10). The Tank circuit consists of an inductance coil in parallel with a capacitor. When this capacitor is charged with the help of a external

voltage source then energy is stored in the capacitor as electrical energy. When external voltage source is removed then capacitor start discharging through inductance coil, and current through inductance coil increases with time. the electrical energy stored at capacitor is converted into magnetic energy.

Due to the change in the magnetic flux associated with inductance coil, an e.m.f. is induced across the ends of inductor in such a way that it opposes the change. When capacitor is completely discharged at that moment induced e.m.f is maximum across the inductor coil. Due to this e.m.f. the capacitor start charging in opposite direction. If there is no energy loss in the circuit then these oscillation will continue for infinite time. But in practice there are energy losses in the circuit due to resistance present in the circuit. So the amplitude of oscillation start decreasing with time.

If energy loss in the circuit could be compensated with the same rate by some external agency then amplitude of oscillation will be constant and oscillation can be maintained.

9.7.1 Barkhausen Criterion

In section 9.6.2 we have discussed the principle of feedback and shown that feedback is called negative when $|1-Ab| > 1$ and it is called positive when $|1-Ab| < 1$. It is evident that with positive feed back the resultant feedback gain $\left(A_f = \frac{A}{(1-A\beta)}\right)$ will be more than the gain of amplifier without feedback (A).

To understand the instability caused by the positive feedback, let us consider that no signal is applied to the amplifier. Let some transient disturbance cause a signal X_0 to appear on the output terminals of the amplifier. If feed back network positive fed back the part of this signal bX_0 to the input terminals of the amplifier then this will appear at the output terminals as increased signal AbX_0. If $AbX_0 = X_0$ then $Ab = 1$ and $A_f = ¥$ then the amplifier will oscillate.

This implies that if we provide positive feedback to an amplifier and make $|Ab|$ almost equal to the unity then amplifier may break into spontaneous oscillations. This is Known as the Barkhausen Criterion.

9.7.2 General Form of Oscillator Circuit

General form of Radio frequency oscillators is shown in Figure (9.11a) .In this circuit active device may be a Transistor, Vacuum Tube, FET or an Operational Amplifier. The linear equivalent circuit with common emitter configuration of a transistor as active device is shown in Figure (9.11 b).

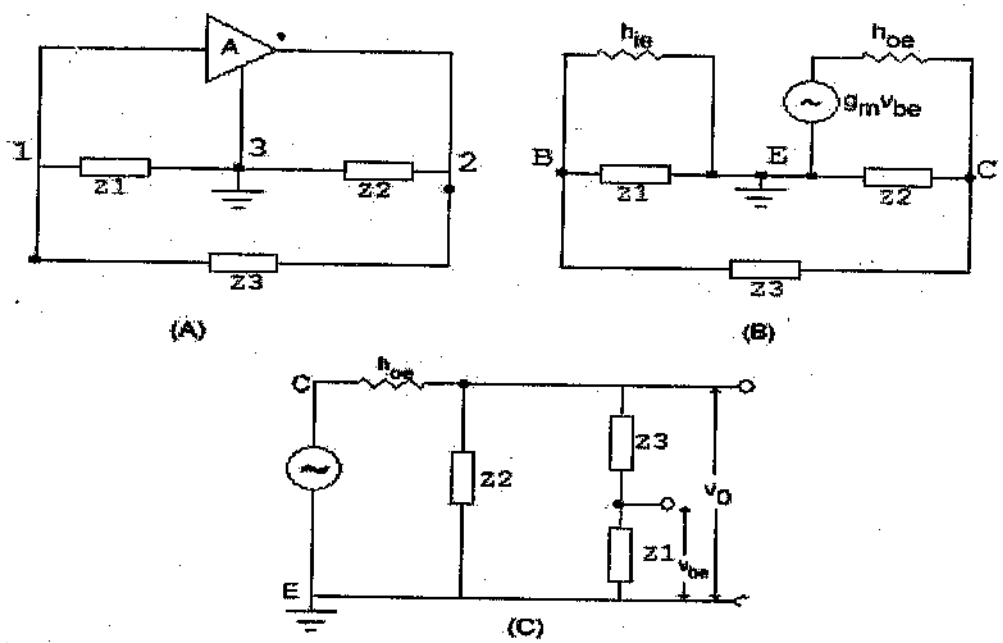


Fig. 9.11 (A) General form of Radio frequency oscillators
(B) The linear equivalent circuit with common emitter configuration of a transistor as active device
(C) Simplified Linear Equivalent Circuit of RF Oscillator

From Figure (9.11 c) it is evident that the impedance Z_1 and Z_3 are in series combination and this combination is parallel to Z_2. Thus the equivalent impedance Z_L will be –

$$Z_L = \frac{Z_2 (Z_1 + Z_3)}{(Z_1 + Z_2 + Z_3)}$$

Current (I) through h_{oe} will be –

$$I = \frac{g_m V_{be}}{h_{oe} + Z_L}$$

Output voltage $V_0 = -I Z_L$

$$V_0 = - g_m V_{be} \frac{Z_L}{h_{oe} + Z_L}$$

Open loop gain of the amplifier

$$A = \frac{V_0}{V_{be}} = - g_m \frac{Z_L}{h_{oe} + Z_L}$$

Feed bac

k voltage $V_f = \frac{V_0}{(Z_1 + Z_3)} Z_1$

Feedback Coefficient $\beta = \frac{V_f}{V_0} = \frac{\frac{Z_1 h_{ie}}{(Z_1 + h_{ie})}}{\left(\frac{Z_1 h_{ie}}{(Z_1 + h_{ie})} + Z_3\right)}$

Neglecting h_{ie} then –

$$\beta = \frac{Z_1}{(Z_1 + Z_3)}$$

Feedback Factor $A\beta = \left(- g_m \frac{Z_L}{h_{oe} + Z_L}\right)\left(\frac{Z_1}{(Z_1 + Z_3)}\right)$

$$= \left(- g_m \frac{\left(\frac{Z_2 (Z_1 + Z_3)}{(Z_1 + Z_2 + Z_3)}\right)}{h_{oe} + \left(\frac{Z_2 (Z_1 + Z_3)}{(Z_1 + Z_2 + Z_3)}\right)} \right)\left(\frac{Z_1}{(Z_1 + Z_3)}\right)$$

$$= -\left(\frac{g_m Z_1 Z_2}{h_{oe}(Z_1 + Z_2 + Z_3) + Z_2 (Z_1 + Z_3)}\right)$$

If the impedances are pure reactance's (either inductive or capacitive) the we can substitute $Z_1 = jX_1$, $Z_2 = jX_2$ and $Z_3 = jX_3$

$$- A\beta = \left(\frac{g_m X_1 X_2}{h_{oe} j(X_1 + X_2 + X_3) - X_2 (X_1 + X_3)}\right)$$

In order that loop gain be real

$X_1 + X_2 + X_3 = 0$

$$-A\beta = \left(-\frac{g_m X_1 X_2}{X_2(X_1+X_3)}\right)$$

$$A\beta = \left(\frac{g_m X_1}{(X_1+X_3)}\right)$$

Thus

$$-A\beta = \left(\frac{g_m X_1}{X_2}\right)$$

For sustained oscillations -Ab must be positive and equal to unity in magnitude. Hence X_1 and X_2 must have same sign. i.e. either both must be inductive or both capacitive. As $X_1+X_2 = -X_3$; this equation indicates that when X_1 and X_2 are inductive then X_3 must be capacitive and vice-versa.
In Hartley Oscillator X_1 and X_2 are inductors and X_3 is capacitor. While in Colpitts Oscillator X_1 and X_2 are capacitors and X_3 is inductor.

9.7.3 Hartley Oscillator

Circuit Diagram of Hartley Oscillator using a transistor in CE- Configuration is shown Figure (9.12) .In this circuit R_E and C_E and combination of resistance R_1 and R_2 provides stabilized self bias. Variable capacitor C and the inductors L_1 and L_2 determine the frequency o f the oscillator. The Coil L_1 is inductively connected with L_2 and the combination acts as an auto-transformer. Inductance coil L_1 is connected between the Base and emitter terminals (Input Circuit) of the CE amplifier, while coil L_2 is connected between the collector and emitter terminals (Output Circuit) of the CE amplifier. The feedback action between output and input circuit is accomplished through transformer action.

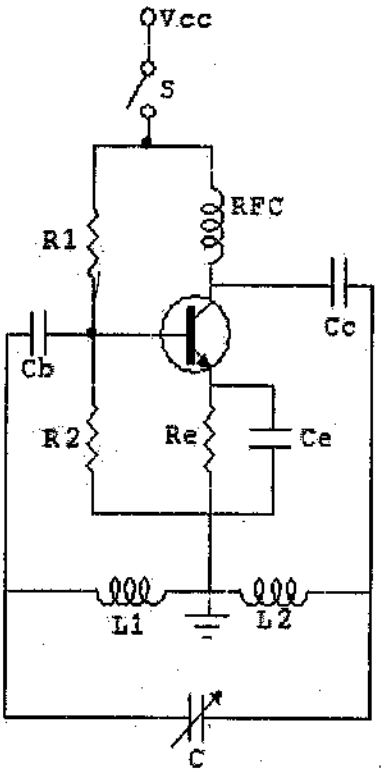


Fig. 9.12 Hartley Oscillator

We know that transformer introduces a phase change of 180° and CE amplifier also introduces a phase change of 180°. Thus the total phase change becomes 360°, which makes the feedback positive.

When switch S is closed then collector current start flowing and charges the capacitor C. When Capacitor C is fully charged then it start discharging through inductance coil L_1 and L_2, which sets the damped harmonic oscillations in the tank circuit. As inductance coil L_1 is connected between the input terminals of the amplifier, so the damped oscillations across L_1 are applied to input circuits and appear as amplified signal in output circuit. Due to the mutual inductance between L_1 and L_2 this output signal is positively fed back to the inputs of the amplifier circuit and energy is continuously supplied to the tank circuit to overcome the losses. The frequency of sustained oscillations of a Hartley Oscillator is given by –

$$f = \frac{1}{2\pi}\frac{1}{\sqrt{\{(L_1+L_2+2M)C\}}}$$

9.7.4 Colpitt's Oscillator

Circuit Diagram of Colpitt's Oscillator is shown Figure (9.13) which is similar to the circuit of Hartley Oscillator except the Inductance coils L_1 and L_2 are replaced by capacitor C_1 and C_2 and variable capacitor is replaced by inductance coil L.

When switch S is closed, capacitors C_1 and C_2 are charged. These capacitor discharge through inductance coil L and setup damped harmonic oscillations in the circuit. As Capacitor C_1 is connected in the input circuit of the amplifier, thus oscillations across C_1 are applied to the input of the amplifier and amplified form appear in output circuit of amplifier across capacitor C_2. The amount of feedback depends upon the relative capacitance of C_1 and C_2.

Capacitor C_1 and C_2 acts as an alternating voltage divider circuit and introduces a phase change of 180° and CE amplifier also introduces a phase change of 180°. Thus the total phase change becomes 360°, which makes the feedback positive. In this way continuous undamped oscillations are produced. The frequency of sustained oscillations of a Colpitt's Oscillator is given by –

$$f = \frac{1}{2\pi}\sqrt{\left\{\frac{(C_1 + C_2)}{LC_1C_2}\right\}}$$

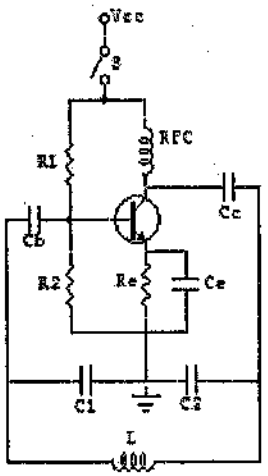


Fig. 9.13 Colpitt's Oscillator

9.8 TRANSISTOR AS A SWITCH

When used as an AC signal amplifier, the transistors Base biasing voltage is applied so that it operates within its "Active" region and the linear part of the output characteristics curves are used. However, both the NPN & PNP type bipolar transistors can be made to operate as an "ON/OFF" type solid state switch for controlling high power devices such as motors, solenoids or lamps. If the circuit uses the Transistor as a Switch, then the biasing is arranged to operate in the output characteristics curves in the areas known as the "Saturation" and "Cut-off" regions as shown in Figure (9.14).

In "Cut-off" region, the operating conditions of the transistor are zero input base current (I_B), zero output collector current (I_C) and maximum collector voltage (V_{CE}) which results in a large depletion layer and no current flows through the device. The transistor is switched "Fully-OFF". In "Saturation" region, the transistor will be biased so that the maximum amount of base current is applied, resulting in maximum collector current flow and minimum collector emitter voltage which results in the depletion layer being as small as possible and maximum current flows through the device. The transistor is switched "Fully-ON". Then we can summarize this as:

1. Cut-off Region - Both junctions are Reverse-biased, Base current is zero or very small resulting in zero Collector current flowing, the device is switched fully "OFF".
2. Saturation Region - Both junctions are Forward-biased, Base current is high enough to give a Collector-Emitter voltage of 0V resulting in maximum Collector current flowing, the device is switched fully "ON".

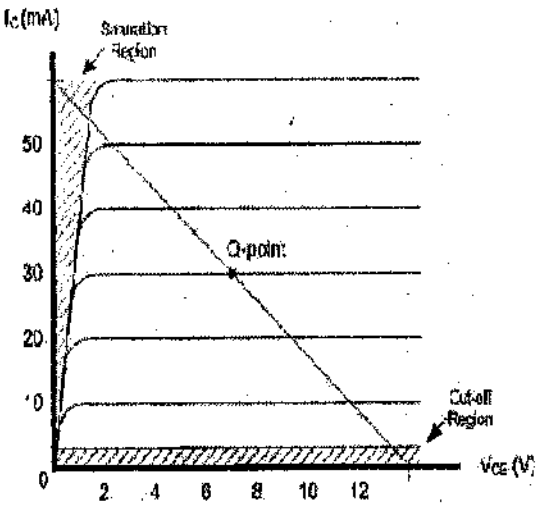


Figure 9.14 Output Characteristic Curves of Transistor

9.9 FIELD EFFECT TRANSISTORS

Junction Field Effect Transistor (JFET) is a three terminal unipolar solid state device. Unlike conventional transistor, FET pertain depend upon flow of majority charge carriers. In FET the current is controlled by an electric field. FET's are of two types –

(i) Junction field effect transistor (JFET)

(ii) Metal-oxide Semiconductor FET (MOSFET)

9.9.1 Construction

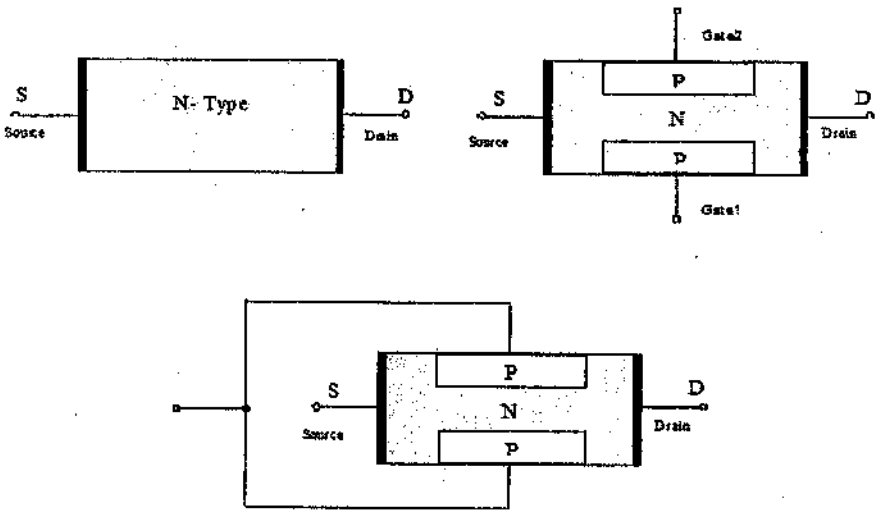


Fig. 9.16 N-Channel Junction Field Effect Transistor

(A) (B)

Fig. 9.16 (A) Circuit Symbol of N-Channel JFET
(B) Circuit Symbol of P-Channel JFET

A JFET can be of N-Channel type or of P-channel type. We will discuss the construction of N-channel JFET. The structure of the N-channel JFET starts with a bar of N-type silicon. Ohmic contacts are made at the two ends of the bar. The bar behaves like a resistor between its two terminals. The two terminals are called Source and Drain (Figure 9.15 a). Two P-type junctions are diffused on opposite sides of its middle part. These P regions are called Gates (Figure 9.15 b). The two gates are internally connected together. The area between these gates is called channel (Figure 9.15 c).
Circuit Symbol of N-Channel and P-Channel JFET is shown in Figure (9.16 a) and (9.16 b) respectively.

9.9.2 Opertion

Biasing circuit of N-Channel and P-Jhannel JFET is shown in Figure (9.17a) and (9.17 b). Normally, a N-Channel JFET is operated by applying positive voltage to the drain with respect to the source. Due to positive voltage the majority carriers (electrons) start drifting from source to the drain. The flow of electrons makes the drains current I_D. These electrons pass through the space between the two P regions, known as channel. The width of the channel can be controlled by varying the gate voltage.

Due to reverse bias is applied to the gate, the width of the depletion region increases. As N-type bar is lightly doped in comparison to the P-type region, the depletion region is more extended into the N-type bar. Thus, reverse bias to the gate reduces the width of the channel and increases its resistance. This reduces the drain current I_D. The shape of the channel is narrower at the drain end, because the reverse bias is not same throughout the length of the PN-junction. The reverse bias between gate and the drain end of the bar is more in comparison to the gate and source end.
When reverse gate bias is further increased, the channel becomes narrower at the drain end and drain current further reduced. When reverse gate bias is sufficiently large then depletion regions will extend

into channel and meet. This pinches-off the drain current and the gate-source voltage at which Pinch-off occurs is known as pinch-off voltage V_P. At pinch-off voltage V_P the channel width reduces to constant minimum value and drain current flows through this constricted channel.

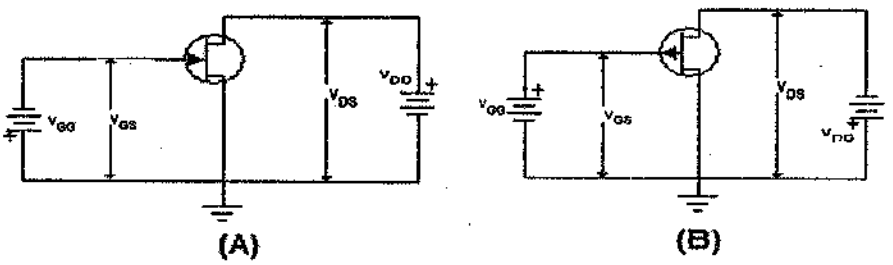


Fig. 9.17 (A) Biasing of N-Channel JFET
(B) Biasing of P-Channel JFET

9.9.3 Characteristic Curves

In previous section we have seen that the drain current I_D depends upon the drain source voltage V_{DS} and gate source voltage V_{GS}. The curves showing the dependence of one quantity over other are called characteristic curves of JFET.

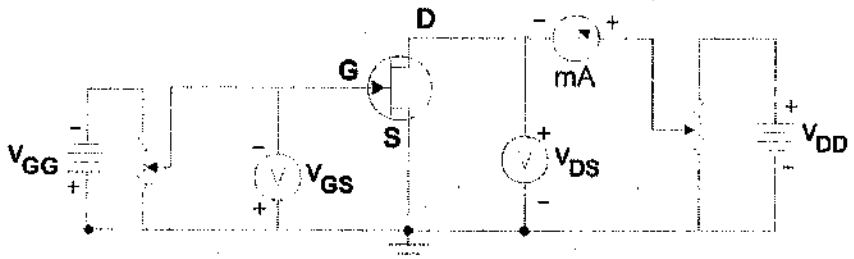


Figure 9.18 Circuit to determine JFET Characteristics

The curve showing the dependence of drain current I_D with drain source voltage V_{DS} at a constant gate-source voltage V_{GS} are called drain characteristic curves and curves showing the dependence of drain current with gate-source voltage V_{GS} at a constant drain source voltage V_{DS} are known as transfer characteristic curves. The circuit diagram for studying characteristics curves of a JFET is shown in Figure (9.18).

9.9.3.1 Drain Charcteristic Curves

Drain characteristic curves are shown in Figure (9.19) When $V_{GS} = 0$, the channel is fully open. For $V_{DS} = 0$, there will be no attracting potential at the drain so no electron from source will reach to the drain and drain current will be zero. When, V_{DS} is increased slightly then N-type bar acts as a semiconductor and drain current I_D increases linearly with V_{DS}. When the voltage V_{DS} further increased then a value of V_{DS} is reached at which the channel is pinched off. With further increase in V_{DS} the current I_D approaches to a constant value.

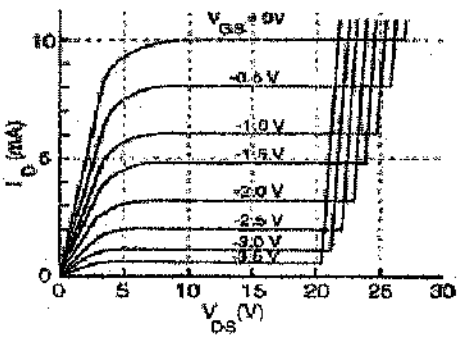


Figure 9.19 Drin Charcteristics Curve of JFET

Continuous increase of V_{DS} causes avalanche breakdown across the gate junctions and high drain current I_D flows in the circuit

9.9.3.2 Transfer Charcteristic Curves

For a given value of V_{DS} the transfer characteristic curves are shown in Figure (9.20). From these curve it is clear that for a definite value of reverse voltage V_{GS} the drain current is zero. This specific value of V_{GS} is known as cut-off voltage. The tangent drawn on the curve at $V_{GS}=0$, on being extended, it cuts the x-axis at $V_{GS} = -V_P/2$. The transfer characteristic can be represented by the following equation--

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Where I_{DSS} is the saturated drain current when $V_{GS}=0$

9.10 SUMMARY

- The ratio of output current to input current of a transistor amplifier is known as current gain (A_i).
- Input impedance of a transistor amplifier is the impedance reflected at the input terminal and it is equal to the ratio of input voltage to input current.
- The ratio of output voltage and input voltage is known as voltage gain (A_v) of the transistor amplifier.
- Ratio of Voltage V_2 and current I_2 is called output Impedance Z_0.
- The ratio of output power and input power is known as power gain (A_p) of the transistor amplifier.
- Feedback is a process in which a fraction of output energy is fed back to input.
- When, Input signal and feedback signal are in same phase, then magnitude of input signal increases by addition of feedback signal. This type of feedback is known as positive feedback or regenerative feedback.
- When, Input signal and feedback signal are in opposite phase then the magnitude of input signal decreases. This type of feedback is known as negative feedback or degenerative feedback.
- All feedback circuit can be classified in following four categories: (i) Voltage Series Feedback (ii) Voltage Shunt Feedback (iii) Current Series Feedback (iv) Current Shunt Feedback
- If $|1 - A\hat{a}| > 1$ i.e. $A\hat{a}$ is negative, then $|A_f| < |A|$. This type of feedback is called negative feedback.
- If $|1 - A\hat{a}| = 0$ i.e. $A\hat{a}=1$ then $|A_f| =$ ".
- If $|1 - A\hat{a}| < 1$ i.e. $A\hat{a}$ is Positive, then $|A_f| > |A|$. This type of feedback is called positive feedback.
- The oscillator may be defined as a circuit which generates an A.C. output signal without externally applied input signal or it is a circuit which converts DC energy into AC energy at very high frequency.
- If we provide positive feedback to an amplifier and make $|Ab|$ almost equal to the unity then amplifier may break into spontaneous oscillations. This is Known as the Barkhausen Criterion.
- For sustained oscillations -Ab must be positive and equal to unity in magnitude. Hence X_1 and X_2 must have same sign. i.e. either both must be inductive or both capacitive. when X_1 and X_2 are inductive then X_3 must be capacitive and vice-versa.
- In Hartley Oscillator feedback action between output and input circuit is accomplished through transformer action and CE amplifier also introduces a phase change of 180°. Thus the total phase change becomes 360°, which makes the feedback positive.
- In colpitt's oscillator Capacitor C_1 and C_2 acts as an alternating voltage divider circuit and introduces a phase change of 180° and CE amplifier also introduces a phase change of 180°. Thus the total phase change becomes 360°, which makes the feedback positive.
- In "Cut-off" region, the operating conditions of the transistor are zero input base current (I_B), zero output collector current (I_c) and maximum collector voltage (V_{CE}) which results in a large depletion layer and no current flows through the device. The transistor is switched "Fully-OFF".

9.11 REVIEW QUESTION

Q.1. Describe the action of a trnsistor as an amplifier. Derive expressions for current gain, Voltage gain, Input impedence and outputimpedence in terms of h parameteters.

Q.2. Explain the concept of load line and Quiescent point.

Q.3. What do you mean by biasing of Bipolar junction transistor? Draw the circuit diagram of fixed bias and self emitter feedback cicuit and explain their working.

Q.4. What do you mean by feedback? Explain different techniques used for feedback in an amplifier.

Q.5. Draw the block diagram of a negative feedback amplifier amplifier and obtain the expression for its closed loop gain.

Q.6. What do you mean by Oscillator?Explain the working of tank circuit.
Q.7. Describe Barkhausen criterion.
Q.8. Draw the circuit diagrm of a general oscillator and obtain the maintenance condition of the oscillator.
Q.9. Draw the circuit digrm of Hartely Oscillator and explain its working.
Q.10. Draw the circuit digrm of Colpit Oscillator and explain its working.
Q.11. Explain the working of a trnsistor as a switch.
Q.12. Describe the construction of a junction field effect transistor.
Q.13. Draw cicuit diagram for studying the characteristic curves of a JFET and explain the drain and transfer characteristic curves of a JFET.
Q.14. Draw the biasing circuit of a N-channel JFET and explain the operation of a JFET.

Unit-10
LOGIC GATES

10.0 OBJECTIVE

In this chapter we will discuss –

- Study of Number System
- Commonly used Number System like Decimal, Binary, Octal and Hexadecimal Number System
- Inter-conversion from one Number system to another Number System
- Binary Arithmetic
- 1's compliment and 2's compliment representation
- Logic Gates - Symbol, Truth table

- Exclusive OR and NOR gates
- Representation of Logic functions
- Realization of Basic Gates (AND, OR and NOT) using NAND and NOR gates.

10.1 NUMBER SYSTEMS

A number system is the set of symbols used to express quantities as the basis for counting, determining order, comparing amounts, performing calculations, and representing value. It is the set of symbols known as digit with mathematical rules that are used to represent a number and performing arithmetic operations like addition, subtraction, multiplication etc. Number of different distinct digits, which can occur in each position in number system, is known as **Base or Radix** of that number system. Generally, a number has two parts- integer part and fractional part which are separated by a radix point (.). A number can be represented as –

$$(N)_B = D_{M-1} D_{M-2} \ldots D_1 D_0 \;.\; D_{-1} D_{-2} \ldots D_{-K}$$

(Integer Part) (RadixPoint) (Fractional Part)

Where N = *A Number*

B = *Radix or Base of the number System*

M = *Number of Digits in Integer Part*

K = *Number of Digits in Fractional Part*

D_{M-1} = *Most Significant digit (MSD)*

D_{-K} = *Least Significant digit (LSD)*

In a Number system the absolute value of digit is fixed but its position value or place value or weight is determined by its position in the Number. For example, the number $(3567.435)_{10}$ can be written as-

$$(3567.435)_{10} = 3\times10^3 + 5\times10^2 + 6\times10^1 + 7\times10^0 + 4\times10^{-1} + 3\times10^{-2} + 5\times10^{-3}$$

Similarly, the number $(1011.001)_2$ can be written as –

$$(1011.001)_2 = 1\times2^3 + 0\times2^2 + 1\times2^1 + 1\times2^0 + 0\times2^{-1} + 0\times2^{-2} + 1\times2^{-3}$$

There are four number systems are often used –

(i) Digital Number System
(ii) Binary Number System
(iii) Octal umber System
(iv) Hexadecimal Number System

10.2 DECIMAL NUMBER SYSTEM

Decimal Number system is well known and widely used number system. The Base or Radix of this number system is 10. It has ten distinct digits:

0, 1, 2, 3, 4, 5, 6, 7, 8, 9

In this number system integer part and fractional part of number are separated by a decimal point (.). In this number system the position value/weights are found by raising the base of number system to power of the position. For integer part of the number, powers are numbered to left of the decimal point starting with 0 and for fractional part of the number, powers are numbered to the right of decimal point starting with -1.For example number $(1243.658)_{10}$ can be written as –

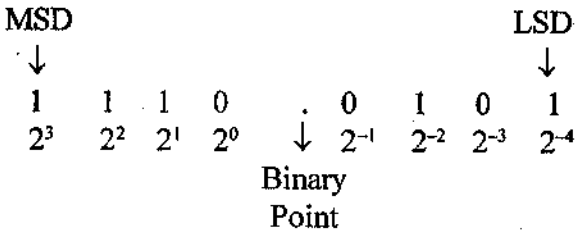
$$(1243.658)_{10} = 1\times10^3 + 2\times10^2 + 4\times10^1 + 3\times10^0 + 6\times10^{-1} + 5\times10^{-2} + 8\times10^{-3}$$

10.3 BINARY NUMBER SYSTEM

In 1854, George Boole proposed binary number system. This is a mathematical system of Logic. Base or Radix of this number system is 2. In this number system there are two variables – True and

False. Numeric symbol of these variables is 1 and 0 respectively. In each binary number the position value or weight of each bit increases in powers 2 starting with 0 to the left of the binary point and decreases to the right of the binary point starting with power of -1.

The weight of each bit of a 8-bit number $(1110.0101)_2$ is as follows:



10.3.1 Binary to Decimal Conversion

The decimal equivalent of the binary number may be obtained as follows-

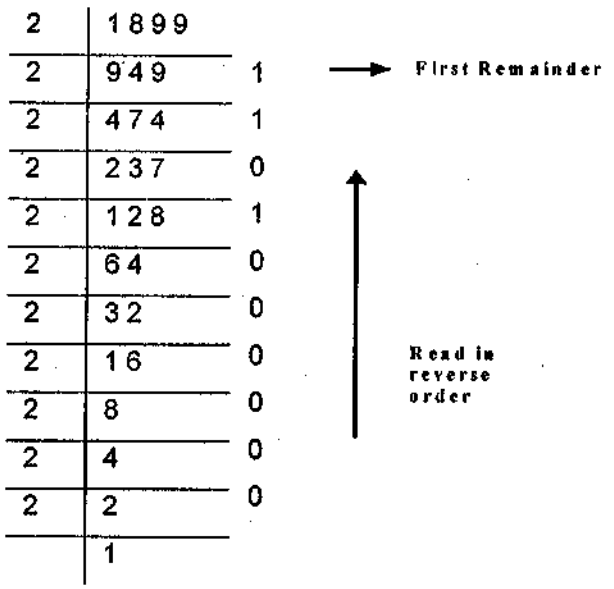
$$(1110.0101)_2 = (1\times2^3)+(1\times2^2)+(1\times2^1)+(0\times2^0)+(0\times2^{-1})+(1\times2^{-2})+(0\times2^{-3})+(1\times2^{-4})$$

$$= 8+4+2+0+0+0.25+0+0.0625$$

$$= 14.3125$$

10.3.2 Decimal to Binary Conversion

For Decimal to Binary conversion, given decimal is successively divided by 2, giving succession remainders of 0 or 1. The reminder reads in reverse order gives the binary equivalent of decimal number. The binary equivalent of decimal number $(1899)_{10}$ can be obtained as follows:



$$(1899)_{10} = (10000001011)_2$$

10.4 SIGNED BINARY SYSTEM

In Decimal number system a plus (+) sign is used as prefix to represent a positive number while (-) sign is used as prefix to represent a negative number. In practice, plus sign is usually dropped and the absence of any sign indicates that number is a positive number. This representation of number is known as **Signed Number**.

To represent the sign in binary number an additional bit is used as the sign bit and it is placed as the most significant bit. If most significant bit is zero then number is positive and if it is one then number is negative. For example – 8 signed binary number $(01011101)_2$ is a positive number and its decimal equivalent value is $(01011101)_2 = (+93)_{10}$ and $(11011101)_2$ is a negative number with decimal value

$(01011101)_2 = (-93)_{10}$.

10.5 BINARY ARITHMETIC

We are familiar with the arithmetic operation like addition, subtraction, multiplication and division in Decimal Number system. Similar Arithmetic operation can be performed in Binary Number System

10.5.1 Binary Addition

Rules for binary addition are as follows:

$0 + 0 = 0$
$1 + 0 = 1$
$0 + 1 = 1$
$1 + 1 = 10$ *i.e.* 0 with carry over of 1

For example, binary addition of binary numbers $(111010)_2$ and $(100101)_2$ will be-

```
  111010
+ 100101
--------
 1011111
--------
```

10.5.2 Binary Subtraction

Following rules apply in binary subtraction:

$0 - 0 = 0$
$1 - 0 = 1$
$10 - 1 = 1$
$1 - 1 = 0$

For example, binary subtraction of binary numbers $(1110.10)_2$ and $(1001.01)_2$ will be

```
  1110.10
+ 1001.01
---------
  0101.01
---------
```

10.5.3 Binary Multiplication

Method of binary multiplication of two binary numbers is similar to the method of multiplication of two decimal numbers. For example, binary multiplication of two binary numbers $(110.10)_2$ and $(100.01)_2$ will be –

```
    110.01
  ×100.01
----------
    11001
   00000×
  00000××
 00000×××
11001××××
----------
 11010.1001
----------
```

10.5.4 Binary Division

Similar to binary multiplication, Method of binary number division is same as the method of decimal number division. For example, binary division of two binary numbers $(1111001)_2$ and $(1001)_2$ will be –

```
1101.0111
```

```
1001 | 1111001
       1001
       -----
       01100
        1001
       -----
       01101
        1001
       -----
       10000
        1001
       -----
       01110
        1001
       -----
        1010
        1001
       -----
          01
```

$(1111001)_2 ,(1001)_2 = (1101.0111)_2$

10.6 1's COMPLIMENT REPRESENTATION

In a binary number, if each 1 is replaced by 1 and each 0 is replaced by 1, then the resulting number is said to be 1's compliment. If binary number is signed binary number then 1's compliment of positive number will be a negative number with same value and vice-versa. For example –

1's compliment of the Binary Number $(11011110)_2$ is $(00100001)_2$.

Similarly, 1's compliment of signed decimal number +20 and -20 is $(010100)_2$ and $(1\ 10100)_2$ respectively.

10.6.1 Subtraction Using 1's Compliment

Binary subtraction can be performed by adding 1's compliment of the subtrahend to minuend. If final carry is generated then add it to get the final answer. e.g. subtract $(1001)_2$ from $(1011)_2$.

```
  1 0 1 1
+ 0 1 1 0      ← 1's compliment of subtrahend.□
1 0 0 0 1
        1
  0 0 1 0
```

10.7 2's COMPLIMENT REPRESENTATION

If a 1 is added to the 1's compliment of a binary number then the resultant binary number is said to be 2's compliment of that binary number. i.e.

2's compliment = 1's compliment + 1

1's compliment of the Binary Number $(11011110)_2$ is $(00100001)_2$.

2's compliment of the Binary Number $(11011110)_2$ will be $(00100001)_2 + 1 = (00100010)_2$

10.7.1 Subtraction Using 2's Compliment

Binary subtraction can be performed by adding 1's compliment of the subtrahend to minuend. If final carry is generated then drop it to get the final answer. e.g. subtract $(1001)_2$ from $(1011)_2$.

```
  1 0 1 1
+ 0 1 1 1     2's compliment of subtrahend
1 0 0 1 0
Carry is ↵
dropped      = 353.4414
  0 0 1 0
```

10.8 OCTAL NUMBER SYSTEM

Base or radix of octal number system is 8 which mean that it has eight distinct counting digits:

0, 1, 2, 3, 4, 5, 6 and 7

Similar, to Decimal and Binary number systems, it is also a positional system and has two parts- integer and fractional which are separated by a radix (octal) point (.).The position value or weight for each digit is given by different powers of 8. The equivalence between 3-bit binary number and octal number is show in Table (10.1).

Table – 10.1

3-Bit Binary	Octal
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

10.8.1 Decimal to Octal Conversion

Decimal to octal conversion can be done by successively dividing by 8, giving succession remainders lying between 0 and 7. The remainder written in reverse order gives the octal equivalent to Decimal Number. *e.g.* $(463)_{10} = (?)_8$.

8 | 463		
8 | 57	7	↑
7	1	↑

$$(463)_{10} = (717)_8$$

10.8.2 Octal to Decimal Conversion

The decimal equivalent of the octal number may be obtained as-

$$(541.342)_8 = \left(5\times8^2\right) + \left(4\times8^1\right) + \left(1\times8^0\right) + \left(3\times8^{-1}\right) + \left(4\times8^{-2}\right) + \left(2\times8^{-3}\right)$$

$$= 320+32+1+\frac{3}{8}+\frac{4}{64}+\frac{2}{512}$$

10.8.3 Binary to Octal Conversion

The conversion of binary number to an octal number can be done by grouping binary number into group of 3 bits starting from right and replace each group by its decimal equivalent shown in table 10.1.e.g.

$$(11101101\ )_2 = \underset{3}{011}\ \underset{5}{101}\ \underset{5}{101} = (355\ )_8$$

10.8.4 Octal to Binary Conversion

The conversion of octal number to an binary number can be done by replacing each octal digit by its 3-bit binary equivalent shown in table 10.1.e.g.

$$(3561)_8 = \underset{3}{011}\ \underset{5}{101}\ \underset{6}{110}\ \underset{1}{001} = (1110111001)_2$$

10.9 HEXADECIMAL NUMBER SYSTEM

Hexadecimal number system is used to specify addresses of different memory location in computer. The base or radix of this number system is 16. It uses sixteen distinct counting digits 0 through 9 and A to F. In this number system place value or weight for each digit is in ascending powers of 16 fo integers and descending powers of 16 for fractions. The Table 10.2 shows the equivalent hexadecima binary and decimal digits.

Table – 10.2							
Hexadecimal	**Binary**	**Decimal**	**Octal**	**Hexadecimal**	**Binary**	**Decimal**	**Octal**
0	0000	0	0	8	1000	8	10
1	0001	1	1	9	1001	9	11
2	0010	2	2	A	1010	10	12
3	0011	3	3	B	1011	11	13
4	0100	4	4	C	1100	12	14
5	0101	5	5	D	1101	13	15
6	0110	6	6	E	1110	14	16
7	0111	7	7	F	1111	15	17

10.9.1 Decimal to Hexadecimal Conversion

Decimal to Hexadecimal conversion can be done by successively dividing by 16, giving succession remainders lying between 0 and 15 which are renamed in hexadecimal. The remainder written in reverse order gives the Hexadecimal equivalent to Decimal Number. *e.g.* $(463)_{10} = (?)_{16}$

16	463	
16	28	15 (F)
	1	12(C)

$(463)_{10} = (1CF)_{16}$

10.9.2 Hexadecimal to Decimal Conversion

The decimal equivalent of the Hexadecimal number may be obtained as-

$$(B3D7)_{16} = \left(11\times16^3\right) + \left(3\times16^2\right) + \left(13\times16^1\right) + \left(7\times16^0\right)$$

$$= 11\times4096+3\times256+13\times16+7$$

$$=(46039)_{10}$$

10.9.3 Binary to Hexadecimal Conversion

The conversion of binary number to an Hexadecimal number can be done by grouping binary number into group of 4 bits starting from right and replace each group by its Hexadecimal equivalent shown in table 10.2.e.g.

$$(11101101)_2 = \underbrace{1110}_{E}\ \underbrace{1101}_{D} = (ED)_{16}$$

10.9.4 Hexadecimal to Binary Conversion

The conversion of Hexadecimal number to an binary number can be done by replacing each Hexadecimal digit by its 4-bit binary equivalent shown in Table (10.2).e.g.

$$(3E5F)_8 = \underbrace{0011}_{3}\ \underbrace{1110}_{E}\ \underbrace{0101}_{5}\ \underbrace{1111}_{F}$$

$$= (0011111001011111)_2$$

10.10 AND, OR, NOT, NAND, NOR GATES

10.10.1 AND Gate

The AND gate is a logic device which has two or more inputs and one output. The schematic symbol for 3- input AND Gate is shown in Figure (10.1).

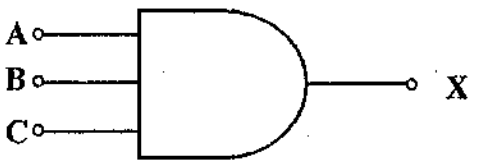


Figure 10.1: Symbol of 3-Input AND gate.

The AND gate produces logic 1 state (High State) at output when all the inputs are in logic state 1 (High State). In Boolean expressions AND operation is represented by dot (.). For example, If A, B and C are three inputs of a AND gate then the output (X) of the AND gate will be represented by following Boolean expression-

$$X = A \cdot B \cdot C \quad OR \quad X = ABC$$

The truth table of 3-input AND Gate is as follows:

INPUT			OUTPUT
A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
1	0	0	0
1	1	0	0
1	0	1	0
0	1	1	0
1	1	1	1

10.10.2 OR Gate

The OR gate is a logic device which has two or more inputs and one output. The schematic symbol for 3- input OR Gate is shown in Figure (10.2).

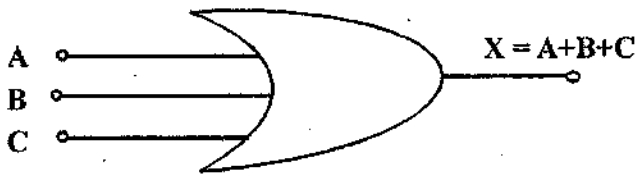


Figure 10.2: Symbol of 3-input OR gate.

The OR gate produces logic 1 state (High State) at output when one of the inputs are in logic state 1 (High State). In Boolean expressions OR operation is represented by plus (+). For example, If A, B and C are three Input of a OR gate then the output (X) of a OR gate will be represented by following Boolean expression-

$$X = A + B + C$$

The truth table of 3-input OR Gate is as follows:

INPUT			OUTPUT
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
1	0	0	1
1	1	0	1
1	0	1	1
0	1	1	1
1	1	1	1

10.10.3 NOT Gate or Inverter

The NOT gate is a logic device which has one input and one output. The schematic symbol for NOT Gate is shown in Figure (10.3).

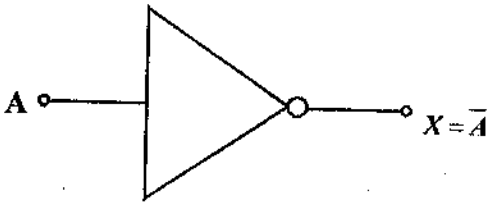


Figure 10.3: Symbol of NOT gate.

The NOT gate produces logic 1 state (High State) at output when input is at logic state 0 (Low State) and Logic 0 state (Low State) at output when input is logic state 1 (High State). All it does is to invert (or compliment) the input. In Boolean expressions inversion or negation or complementation is represented by bar or dash over the function. If A is input of a NOT gate then output (X) of the NOT gate will be represented by following Boolean expression –

$X = \overline{A}$ *OR* $X = A'$

The truth table of a NOT Gate is as follows:

INPUT	OUTPUT
A	X
0	1
1	0

10.11.4 NAND Gate

NAND means NOT+AND. It can be obtained by connecting a NOT gate in the output of an AND gate. The schematic symbol for NAND Gate is shown in Figure (10.4).

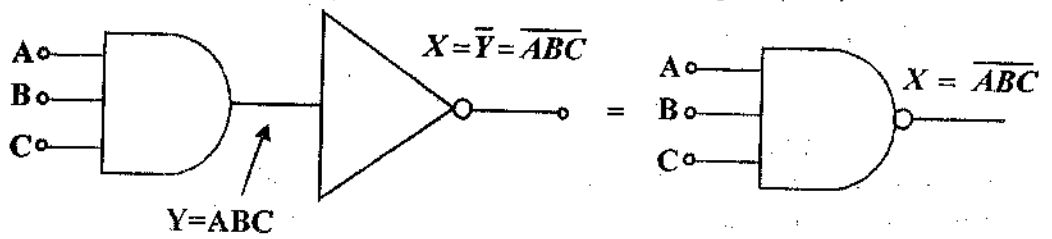


Figure 10.4: Symbol of NAND gate.

The NAND gate produces logic 1 state (High State) at output when all the inputs or one of the inputs are in logic state 0 (Low State) and output is logic 0 state (Low state) when all inputs are logic state 1 (High State). For example, If A, B and C are three inputs of a NAND gate then the output (X) of the NAND gate will be represented by following Boolean expression-

$X = \overline{A \cdot B \cdot C}$ *OR* $X = \overline{ABC}$

The truth table of 3-input NAND Gate is as follows:

INPUT			AND OUTPUT	NAND OUTPUT
A	B	C	Y=ABC	$X = \overline{Y} = \overline{ABC}$
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
1	0	0	0	1
1	1	0	0	1
1	0	1	0	1
0	1	1	0	1
1	1	1	1	0

10.10.5NOR Gate

NAND means NOT+OR. It can be obtained by connecting a NOT gate in the output of an OR gate. The schematic symbol for NOR Gate is shown in Figure (10.5).

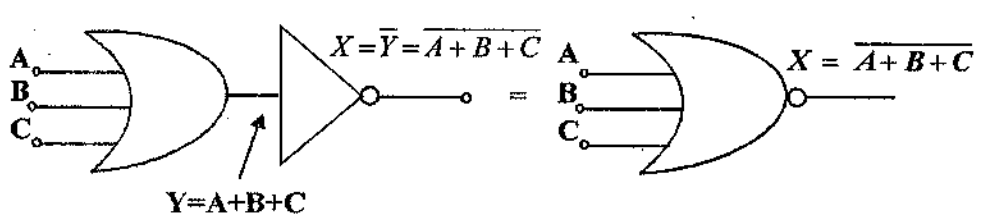


Figure 10.5: Symbol of NOR gate.

The NOR gate produces logic 1 state (High State) at output when all the inputs are in logic state 0 (Low State) and output is logic 0 state (Low state) when all inputs or any of the inputs are in logic state 1 (High State). For example, If A, B and C are three inputs of a NOR gate then the output (X) of the NORgate will be represented by following Boolean expression-

$$X = \overline{A+B+C}$$

The truth table of 3-input NOR Gate is as follows:

INPUT			OR OUTPUT	NOR OUTPUT
A	B	C	Y=A+B+C	$X = \overline{Y} = \overline{A+B+C}$
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
1	0	0	1	0
1	1	0	1	0
1	0	1	1	0
0	1	1	1	0
1	1	1	1	0

10.11 EXCLUSIVE – OR AND EXCLUSIVE – NOR GATES

10.11.1 Exclusive – OR gate

Exclusive OR gate is abbreviated as XOR gate. The schematic symbol for XOR Gate is shown in Figure (10.6).

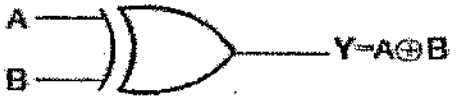


Figure 10.6: Symbol of XOR gate

The XOR gate produces logic 0 state (Low State) at output when all of the inputs are in same state i.e. all inputs are in logic state 1 (High State) or Logic state 0 (Low State) and it produces logic 1 state (High State) at output, when its inputs are different. In Boolean expressions XOR operation is represented by plus ($\oplus$). For example, If A and B two Input of a XOR gate then the output (X) of a XOR gate will be represented by following Boolean expression-

$$X = A \oplus B$$

The truth table of 2-input XOR Gate is as follows:

INPUT		NOR OUTPUT
A	B	$Y = \overline{A \oplus B}$
0	0	0
0	1	1
1	0	1
1	1	0

10.12.2 Exclusive – NOR gate

Exclusive NOR gate is abbreviated as XOR gate. The schematic symbol for XNOR Gate is shown in Figure (10.7).

Figure 10.7: Symbol of XNOR gate

The XNOR gate produces logic 1 state (High State) at output when all of the inputs are in same state i.e. all inputs are in logic state 1 (High State) or Logic state 0 (Low State) and it produces logic 0 state (Low State) at output, when its inputs are different. In Boolean expressions XOR operation is represented by plus ($\oplus$). For example, If A and B two Input of a XOR gate then the output (X) of a XOR gate will be represented by following Boolean expression-

$$X = \overline{A \oplus B}$$

The truth table of 2-input XNOR Gate is as follows:

INPUT		OUTPUT
A	B	$Y = A \oplus B$
0	0	1
0	1	0
1	0	0
1	1	1

10.12 NAND–NOR IMPLEMENTATIONS OF BASIC GATES

NAND and NOR gate is known as Universal gates. Because, by using NAND/ NOR gate we can realize the basic gates- AND, OR and NOT gates.

10.12.1 Realization of basic gates by using NAND gate

Realization of NOT gate using NAND gate is shown in Figure (10.8).

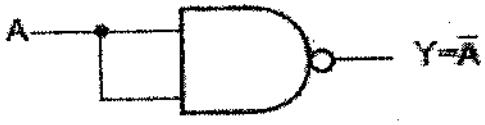


Figure :10.8

Realization of AND gate using NAND gate is shown in Figure (10.9).

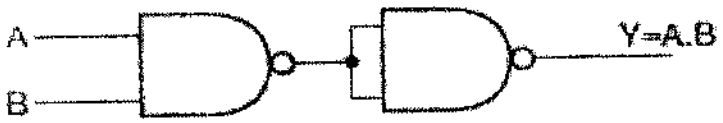


Figure: 10.9

Realization of OR gate using NAND gate is shown in Fig. 10.10 -

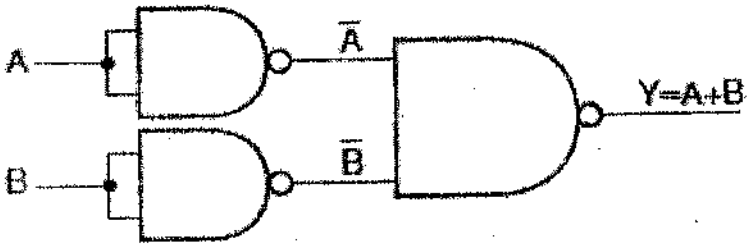


Figure: 10.10

10.12.2 Realization of basic gates by using NOR gate

Realization of NOT gate using NOR gate is shown in Figure (10.11).

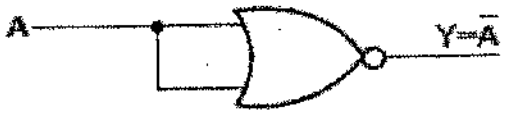


Figure: 10.11

Realization of AND gate using NOR gate is shown in Figure (10.12).

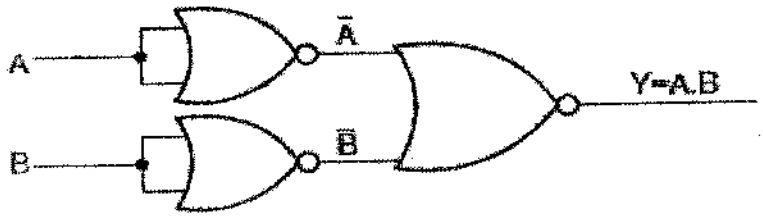


Figure:10.12

Realization of OR gate using NOR gate is shown in Figure (10.13).

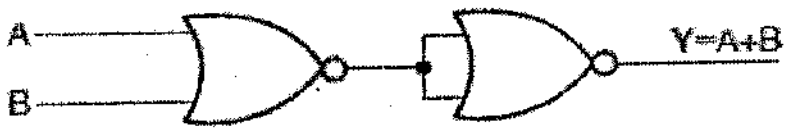


Figure:10.13

10.13 SUMMARY

- A number system is the set of symbols used to express quantities as the basis for counting, deter mining order, comparing amounts, performing calculations, and representing.
- Number of different distinct digits, which can occur in each position in number system, is known as **Base or Radix** of that number system.
- There are four number systems are often used –

(i) Digital Number System (ii) Binary Number System (iii) Octal umber System
(iv) Hexadecimal Number System

- The Base or Radix of Decimal Number system is 10. It has ten distinct digits (0,1,2,3,4,5,6,7,8,9). It is widely used number system.
- Base or Radix of Binary number system is 2. In this number system there are two variables – True and False. Numeric symbol of these variables is 1 and 0 respectively.
- In a binary number, if each 1 is replaced by 1 and each 0 is replaced by 1, then the resulting number is said to be 1's compliment.
- If a 1 is added to the 1's compliment of a binary number then the resultant binary number is said to be 2's compliment of that binary number.
- Base or radix of octal number system is 8 which mean that it has eight distinct counting digits(0,1,2,3,4,5,6 and 7)
- Hexadecimal number system is used to specify addresses of different memory location in com puter. The base or radix of this number system is 16. It uses sixteen distinct counting digits 0 through 9 and A to F.
- The AND gate is a logic device which has two or more inputs and one output. The AND gate produces logic 1 state (High State) at output when all the inputs are in logic state 1 (High State).
- The OR gate produces logic 1 state (High State) at output when one of the inputs are in logic state 1 (High State).
- The NOT gate is a logic device which has one input and one output. The NOT gate produces logic 1 state (High State) at output when input is at logic state 0 (Low State) and Logic 0 state (Low State) at output when input is logic state 1 (High State).
- The NAND gate produces logic 1 state (High State) at output when all the inputs or one of the inputs are in logic state 0 (Low State) and output is logic 0 state (Low state) when all inputs are logic state 1 (High State).
- The NOR gate produces logic 1 state (High State) at output when all the inputs are in logic state 0 (Low State) and output is logic 0 state (Low state) when all inputs or any of the inputs are in logic state 1 (High State).
- The XOR gate produces logic 0 state (Low State) at output when all of the inputs are in same state i.e. all inputs are in logic state 1 (High State) or Logic state 0 (Low State) and it produces logic 1 state (High State) at output, when its inputs are different.
- The XNOR gate produces logic 1 state (High State) at output when all of the inputs are in same state i.e. all inputs are in logic state 1 (High State) or Logic state 0 (Low State) and it produces logic 0 state (Low State) at output, when its inputs are different.

10.14 REVIEW QUESTIONS

Q.1. What do you mean by number system. Explain the following number system
(a) Decimal (b) Binary (c) Octal (d) Hexadecimal.

Q.2. Convert following decimal numbers into equivalent binary numbers-
(a) $(39)_{10}$ (b) $(157)_{10}$ (c) $(27.88)_{10}$ (d) $(12.25)_{10}$

Q.3. Convert decimal $(53875)_{10}$ into equivalent (a) Binary (b) Octal (c) Hexadecimal number.

Q.4. Convert $(FE5)_{16}$ into equivalent (a) Binary (b) Octal (c) Decimal number.

Q.5. Perform following binary arithmetic operations-
(a) $(1101.11)_2 + (101.11)_2$ (b) $(11011.101)_2 - (1101.11)_2$
(c) $(11.110)_2 \times (100.1)_2$ (d) $(101101)_2 >> (1101.11)_2$

Q.6. Perform following subtraction using 1's compliment arithmetic-
(a) $(0.1001)_2 - (0.0110)_2$ (b) $(0.01111)_2 - (0.01001)_2$

Q.7. Perform following subtraction using 1's compliment arithmetic-
(a) $(01100)_2 - (00011)_2$ (b) $(011.1001)_2 - (0001.1110)_2$

Q.8. What do you mean by logic gates.Explain AND,OR,NOT, NOR and NAND gate. Give circuit symbol and truth table of each logic gates.

Q.9. What do you mean by XOR and XNOR gates.Give circuit symbol and truth table of each gate.

Q.10. Realize following gates using NOR gate-
(a) AND (b) OR (c) NOT

Unit-11
BOOLEAN ALGEBRA

Content of the Unit

11.0 OBJECTIVE

In this chapter we will discuss –

- Logic circuits are the basis for almost all modern digital computer systems.
- To understand operation of computers there is need to understand digital logic and Boolean algebra.
- Fundamentals of Boolean algebra and the basic postulates and theorems are used to simplify the design of electronic logic circuits.
- K-maps can be used for the simplification of Boolean equations.

11.1 INTRODUCTION

Boolean algebra is the algebra of two values. These are usually taken to be 0 and 1, as we shall do here, although false and true or ON and OFF are also in common use. For the purpose of understanding Boolean algebra any Boolean domain of two values will do. It was developed by George Boole in the years around 1840 as a system for mathematical analysis of logic. It resembles the algebra of real numbers, but with the numeric operations of multiplication XY, addition X + Y, and negation "X replaced by the respective logical operations of conjunction $X \wedge Y$, disjunction $X \vee Y$, and complement $\overline{X}$. One can represent any algorithm, or any electronic computer circuit, using a system of Boolean equations. This chapter provides a brief introduction to Boolean algebra, truth tables, canonical representation, of Boolean functions, Boolean function simplification, logic design and K-maps can be used for the simplification of Boolean equations. Number of examples is also given to illustrate how one can reduce complicated Boolean expressions.

11.2 BOOLEAN ALGEBRA

Boolean algebra is a deductive mathematical system closed over the values zero and one (false and true). A *binary operation can defined for a* set of values which accept a pair of Boolean inputs and produces a single Boolean value. For example, the Boolean AND operator accepts two Boolean inputs and produces a single Boolean output (the logical AND of the two inputs). For any given algebra system, there are some initial assumptions, or *postulates*, that the system follows. Boolean algebra is closed under the AND, OR, and NOT operations.

The identity element with respect to • is one and + is zero. There is no identity element with respect to logical NOT. One can deduce additional rules, theorems, and other properties of the system from the following basic laws of Boolean algebra.

Basic Laws of Boolean Algebra

1. **Boolean addition**

It is same as the logical OR operation. The basic rules of Boolean addition are given below:

$$0 + 0 = 0$$
$$1 + 0 = 1$$
$$0 + 1 = 1$$
$$1 + 1 = 1$$
$$A + 0 = A$$
$$A + 1 = 1$$
$$A + A = 1$$
$$A + \bar{A} = 1$$

2. **Boolean multiplication**

It is same as the logical AND operation the basic rules of Boolean multiplication methods are as follows:

$$0 \cdot 0 = 0$$
$$1 \cdot 0 = 0$$
$$0 \cdot 1 = 0$$
$$1 \cdot 1 = 1$$
$$A \cdot 1 = A$$
$$A \cdot 0 = 0$$
$$A \cdot A = A$$
$$A \cdot A = 0$$
$$A = A$$

3. **Properties of Boolean Algebra**

The symbol "•" represents the logical AND operation; e.g., A • B is the result of logically ANDing the Boolean values A and B. When using single letter variable names, this text will drop the "•" symbol; Therefore, AB also represents the logical AND of the variables A and B (we will also call this the *product* of A and B). The symbol "+" represents the logical OR operation; e.g., A + B is the result of logically ORing the Boolean values A and B. (We will also call this the *sum* of A and B.) Logical *complement*, *negation*, or *not*, is a unary operator. This text will use the (¯) symbol to denote logical negation. For example, denotes the logical NOT of A. If several different operators appear in a single Boolean expression, the result of the expression depends on the *precedence* of the operators. We'll use the following precedences (from highest to lowest) for the Boolean operators: parenthesis, logical NOT, logical AND, then logical OR. The logical AND and OR operators are *left associative*. If two operators with the same precedence are adjacent, you must evaluate them from left to right. The logical NOT operation is right associative, although would produce the same result using left or right associativity since it is a unary operator.

Commutative property

Boolean addition is commutative, given by

$$A + B = B + A$$

According to this property, the order of the OR operation conducted on the variables makes no difference. Boolean multiplication is also commutative, given by

$$A \cdot B = B \cdot A$$

This shows that the order of the AND operation conducted on the variables makes no difference.

Associative property

Multiplication (•) and addition (+) are both associative. That is,

$$(A \cdot B) \cdot C = A \cdot (B \cdot C) \text{ and}$$
$$(A + B) + C = A + (B + C)$$

According to this property, both OR and AND operations of several variables results in same, regardless of the grouping of the variables.

Distributive property

The Boolean addition is distributive over Boolean multiplication, given by

$A \cdot (B + C) = (A \cdot B) + (A \cdot C)$ and

$A + (B \cdot C) = (A + B) \cdot (A + C)$

Thus distributive property states that the AND operation (multiplication) of several variables and then the OR operation (addition) of the result with a single variable is equivalent to the OR operation of the single variable with each of several variables and then the AND operation of the sums.

Negation property

For every value A there exists a value such that $A\cdot = 0$ and $A+ = 1$. This value is the logical complement (or NOT) of A.

Absorption law

(i) $A + AB = A$

Proof:

$$A + AB = A \cdot 1 + AB$$
$$= A(1 + B)$$
$$= A \cdot 1$$
$$= A$$

(ii) $A \cdot (A + B) = A$

Proof: $A \cdot (A + B) = A \cdot A + A \cdot B$

$$= A + AB$$
$$= A(1 + B)$$
$$= A \cdot 1$$
$$= A$$

(iii) $A + B = A+B$

(iv) $A \cdot (A + B) = AB$

11.3 DE MORGAN'S THEOREMS

De-Morgan proposed two most important theorems of Boolean algebra. The first theorem states that the compliment of a product is equal to the sum of compliments and the second theorem states that the compliment of a sum is equal to the products of compliments. Mathematically these two theorems can be expressed as

1. First law $(ABCD .....) = A + B + C + D + ...$
2. Second law $(A + B + C + D + ...) = A \cdot B \cdot C \cdot D .....$

These theorems can be proved for any number of variables. For simplicity proof the two variable DeMorgan's theorems is given below.

S.No.	1	2	3	4	5	6	7	8	9	10
	A	B	A	B	A+B	A•B	A+B	A•B	A•B	A+B
1	0	0	1	1	0	0	1	1	1	1
2	0	1	1	0	1	0	0	0	1	1
3	1	0	0	1	1	0	0	0	1	1
4	1	1	0	0	1	1	0	0	0	0

From the above table it is cleared that the values of the column 7 and 8 are equal thus,

$A + B = A\ gB$

Similarly, column 9 and 10 are equal. Therefore,

$A\ gB = A + B$

11.4 BOOLEAN FUNCTION

A Boolean function is an algebraic expression formed using binary constants, binary variables and basic logical operation symbols. A Boolean function is a specific Boolean expression or in other

words a Boolean function (*expression) is* a sequence of zeros, ones, and *literals* separated by Boolean operators. A literal is a primed (negated) or unprimed variable name. For example, consider the following Boolean function F

$$F = AB + C$$

This function computes the logical AND of A and B and then logically ORs this result with C. If A =1, B = 0, and C = 1, then F0 returns the value one (1•0 + 1 = 1).

Another example of a three variable Boolean function is given below:

$$(A + B) \cdot (A + C) \cdot (B + C) = (A + B) \cdot (A + C)$$

This Boolean function is composed of three binary variables A, B, C, Compliment of A and SUM and multiplications. There are three logic operations that constitute the three basic logic operations performed by a digital computer.

1. Conjunction (or logical product) commonly referred to as the AND operation and denoted with the dot (•) symbol between variables.
2. Disjunction (or logical sum) commonly called the OR operation and denoted with the plus (+) symbol between variables
3. Negation (or complementation or inversion) commonly called NOT operation and denoted with the bar (¯) symbol above the variable.

11.5 MINIMIZATION OF BOOLEAN EXPRESSIONS

Boolean expressions can be minimized (simplified) by using the basic rules and theorems of Boolean algebra. Unfortunately, there are no fixed rules one can apply to optimize a given expression. Much like constructing mathematical proofs, an individual's ability to easily do these transformations are usually a function of experience. Simplification of Boolean expressions is demonstrated in the examples no. 1, 2 and 3.

Ex.–1. Simplify the expression AB+BC+BC

Solution: $AB+BC+BC = AB + B(C+C)$

$= AB + B \cdot 1$ (Since C+=1)

$= AB + B$

$= B \cdot (A+1)$ (Since A+1=1)

$= B1$

$= B$

Ex–2. Prove that $A\bar{B} + AB + \bar{A}\bar{B} = A + \bar{B}$

Solution: $A\bar{B} + AB + \bar{A}\bar{B} = AB + \bar{B}(A + \bar{A})$

$= AB + \bar{\bar{B}}$

$= AB + \bar{B}(1+A)$

$= AB + \bar{B} + A\bar{B}$

$= A(B + \bar{\bar{B}}) + \bar{B}$

$= A + \bar{B}$

Ex.–3. Simplify the Boolean expression A+A+B

Solution: $A + A\bar{B} + \bar{A}B = A(1 + \bar{\bar{B}}) + \bar{A}B$

$= A.1 + \bar{A}B$

$= A(1 + B) + \bar{A}B$

$= A + AB + \bar{A}B$

$= A + B(A + \bar{A})$

$= A + B$

11.6 SUM OF PRODUCTS (SOP)

In Boolean algebra the AND operation referred to as a product. The logical sum of two or more logical product terms is called a sum of products expression (SOP). SOP is basically an OR operation of AND operated variables such as:

(i) $F = XY + YZ + ZX$

(ii) $F = XY + Y + ZX$

11.7 PRODUCTS OF SUMS (POS)

An OR function (+sign) is generally used to refer a sum. A product of sums expression is a logical product of two or more logical sum terms (POS). POS is basically an AND operation of OR operated variables such as:

(i) $F = (X+Y)(Y+Z)(Z+)$

(ii) $F = (X+Y+Z)(Z+)$

11.8 MINTERMS

A product term containing all the N variables of a function in either complimented or uncomplimented form is called a Minterm. For example two binary variables A and B are ANDed, the four (2^2=4) possible combinations, are ,B, A and AB. These four terms are referred to as *minterms* or *standard products* where the word product here means the ANDing of these variables. In other words, a minterm is composed of two or more variables or their complements ANDed together.

In general, for n variables there are 2^n minterms designated as m_j where the subscript represents the decimal equivalent of the binary number of the minterm. Table (11.1) shows the 8 minterms for the variables A, B, and C, and their designations.

Table 11.1 : Minterms for 3 variables and their designation

A	B	C	Minterm	Designation
0	0	0	ABC	m_0
0	0	1	ABC	m_1
0	1	0	ABC	m_2
0	1	1	ABC	m_3
1	0	0	ABC	m_4
1	0	1	ABC	m_5
1	1	0	ABC	m_6
1	**1**	**1**	**ABC**	$\mathbf{m_7}$

As shown in the above table (11.1), each minterm is obtained from an ANDed term of n variables with each variable being complemented if the corresponding bit is a logical 0, and uncomplemented if the corresponding bit is logical 1.

11.9 MAXTERMS

A sum term containing all the N variables of a function in either complimented or uncomplimented form is called a Minterm. For example two binary variables A and B are ORed, the four ($2^2 = 4$) possible combinations, are A+B, A+B, A+B and A+B. These four terms are referred to as *maxterms* or *standard products* where the word sum here means the ORing of these variables. In other words, a maxterm is composed of two or more variables or their complements ORed together.

In general, for n variables there are 2^n maxterms designated as M_j where the subscript represents the decimal equivalent of the binary number of the minterm. Table (11.2) shows the 8 maxterms for the variables A, B, and C, and their designations.

As shown in Table (11.2), each maxterm is obtained from an ORed term of n variables with each variable being uncomplemented if the corresponding bit is a logical 0, and complemented if the corresponding bit is logical 1.

Table 11.2 Maxterms for 3 variables and their designation

A	B	C	Maxterm	Designation
0	0	0	A+B+C	M_0
0	0	1	A+B+C	M_1
0	1	0	A+B+C	M_2
0	1	1	A+B+C	M_3
1	0	0	A+B+C	M_4
1	0	1	A+B+C	M_5
1	1	0	A+B+C	M_6
1	**1**	**1**	**A+B+C**	M_7

Two important properties of Boolean algebra state that: Any Boolean function can be expressed as a *sum of minterms* where "sum" means the ORing of the terms. Any Boolean function can be expressed as a *product of maxterms* where "product" means the ANDing of the terms. It implies that a Boolean function can be derived from a given truth table by assigning a minterm to each combination of variables that produces a logical 1 and then ORing all these terms.

11.10 KARNAUGH MAP

Karnaugh map is a pictorial method of grouping together logic expressions with common factors and therefore eliminating unwanted variables. A *Karnaugh map*, hereafter referred to as *K-map*, is a matrix of squares. It can be drawn directly from either minterm (sum-of-products) or maxterm (product-of-sums) Boolean expressions. Drawing a Karnaugh map from the truth table involves an additional step of writing the minterm or maxterm expression depending upon whether it is desired to have a minimized sum-of-products or a minimized product of- sums expression. K-map provides a very powerful method of reducing Boolean expressions to their simplest forms

In general, a Boolean expression with n variables can be represented by a K-map of 2^n squares and each possible input is allotted a square. In the case of a minterm Karnaugh map, '1' is placed in all those squares for which the output is '1', and '0' is placed in all those squares for which the output is '0'. 0s are omitted for simplicity. An 'X' is placed in squares corresponding to 'don't care' conditions. In the case of a maxterm Karnaugh map, a '1' is placed in all those squares for which the output is '0', and a '0' is placed for input entries corresponding to a '1' output. Again, 0s are omitted for simplicity, and an 'X' is placed in squares corresponding to 'don't care' conditions.

One important condition has to be satisfied is that the designation of adjacent rows and adjacent columns should be the same except for one of the literals being complemented. Also, the extreme rows and extreme columns are considered adjacent. In other words the squares in K-maps are arranged in such way so that adjacent squares represent terms which differ by only one variable which appears in one square as a complemented variable and as an uncomplemented variable in an adjacent square.

K-map of Two Variables

Figure (11.1) shown below illustrates a two-variable K-map with four squares where each square represents one combination of the variables and the truth table for the general case of a two variable problem.

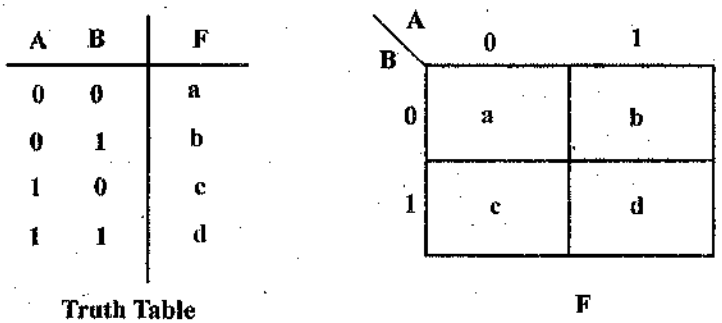


Figure: 11.1 K-map of two variables

n Figure (11.1).

Square **a** represents the combination **A = 0** and **B = 0**, that is, a $\Rightarrow \bar{A}\bar{B}$

Square **b** represents the combination **A = 0** and **B = 1**, that is, b $\Rightarrow \bar{A}B$

Square **c** represents the combination **A = 1** and **B = 0**, that is, c $\Rightarrow A\bar{B}$

Square **d** represents the combination **A = 1** and **B = 1**, that is, d $\Rightarrow AB$

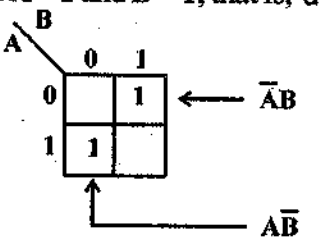


Figure 11.2. K-map for the Boolean expression $C = A\bar{B} + \bar{A}B$

For example, the Boolean expression C = A + B can be shown in a K-map as indicated in Figure (11.2), where the 1s denote the conditions for which the Boolean expression is true (logical 1).

For simplicity, we enter only 1s l in the squares of a K-map and it is understood that all other empty squares contain 0s.

One can also derive a Boolean expression from a K-map. For example, from the K-map shown in Figure (11.3) we derive the Boolean expression $Z = \bar{X}\bar{Y} + XY$.

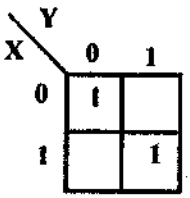


Figure 11.3: K-map for the Boolean expression $Z = \bar{X}\bar{Y} + XY$

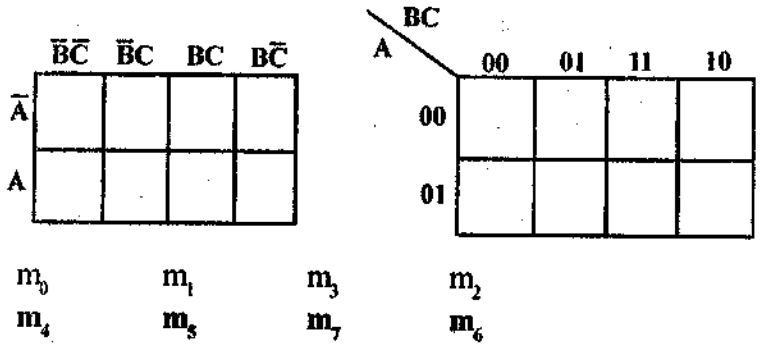
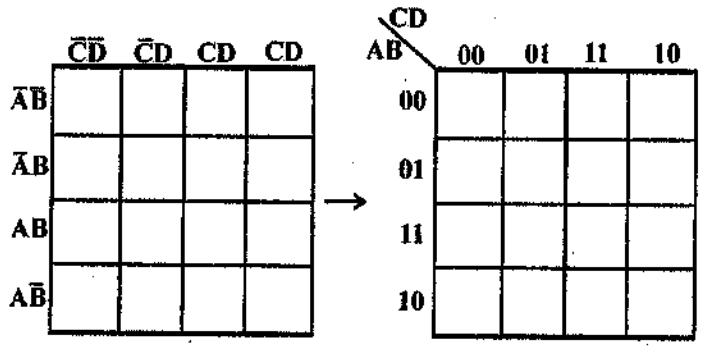


Figure 11.4: Three variable K-maps



m_0	m_1	m_3	m_2
m_4	m_5	m_7	m_6
m_{12}	m_{13}	m_{15}	m_{14}
m_8	m_9	m_{11}	m_{10}

Figure 11.5: Four variable K-maps

It is to be noted that the usefulness of the K-map in simplifying Boolean expressions, the basic property possessed by adjacent squares must be satisfied. Any two adjacent squares in the map are differ by only one variable, which is primed in one square and unprimed in the other. For example, m_1 and m_3 lie in two adjacent squares. Variable y is primed in m_1 and unprimed in m_3, whereas the other two variables are the same in both the squares. From the basics of Boolean algebra, we know that the sum of two minterms in adjacent squares can be simplified to a single AND term consisting of two literals. i.e.

$$m_1 + m_3 = \bar{x}\,\bar{y}\,z + \bar{x}\,y\,z = \bar{x}\,z\,(\bar{y} + y) = \bar{x}\,z$$

Hence the two squares differ by the variable y, which can be removed when the sum of two minterms is formed. Thus, any two minterms in adjacent squares that are ORed together results in removal of the different variable.

11.11 MINIMIZATION

Rules of Simplification

The Karnaugh map uses the following rules for the simplification of expressions by grouping together adjacent cells containing ones.

- **Groups may not include any cell containing a zero**

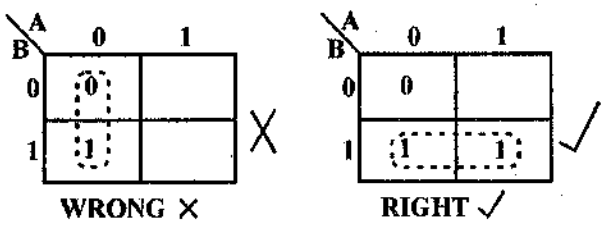


Figure: 11.6

- **Groups may be horizontal or vertical, but not diagonal.**

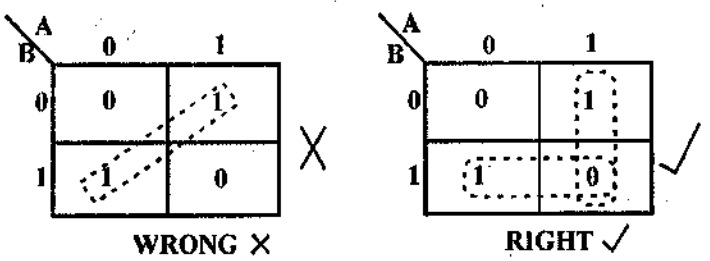


Figure: 11.7

- **Groups must contain 1, 2, 4, 8, or in general 2^n cells.**
  That is if n = 1, a group will contain two 1's since $2^1 = 2$.
- **If n = 2, a group will contain four 1's since $2^2 = 4$.**

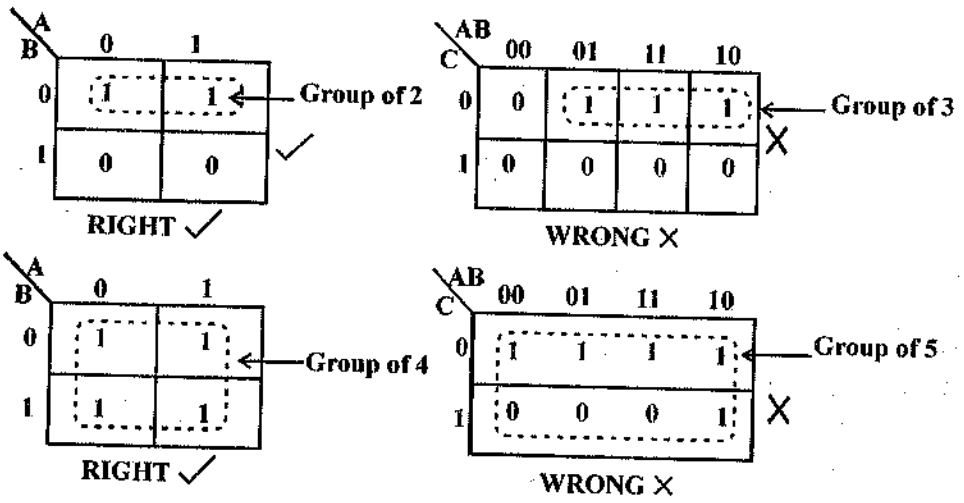


Figure: 11.8

- **Each group should be as large as possible.**

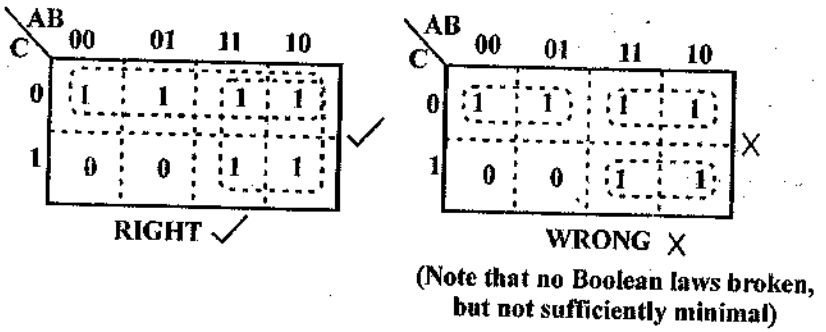


Figure:11.9

- **Each cell containing a one must be in at least one group.**

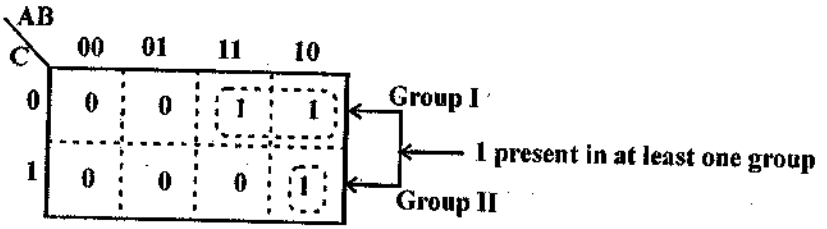


Figure: 11.10

- **Groups may overlap.**

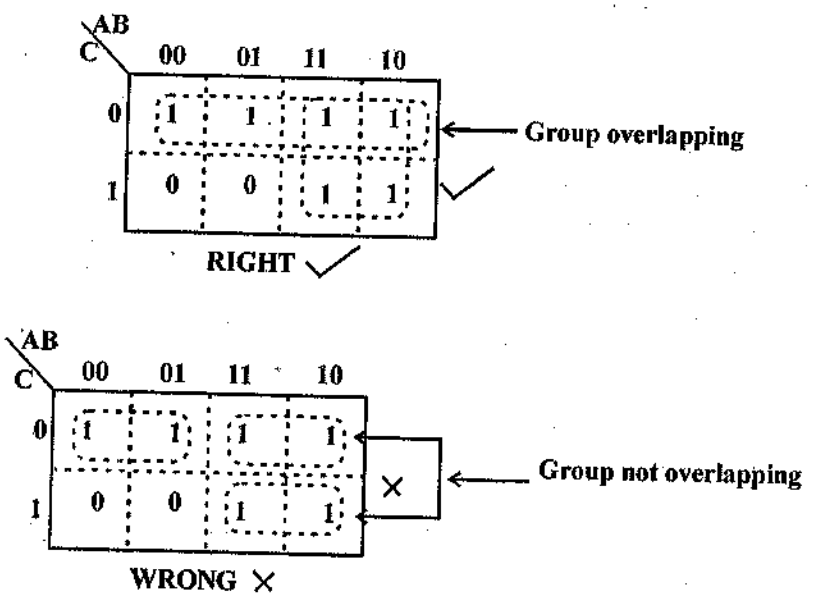


Figure:11.11

- **Groups may wrap around the table. The leftmost cell in a row may be grouped with the rightmost cell and the top cell in a column may be grouped with the bottom cell.**

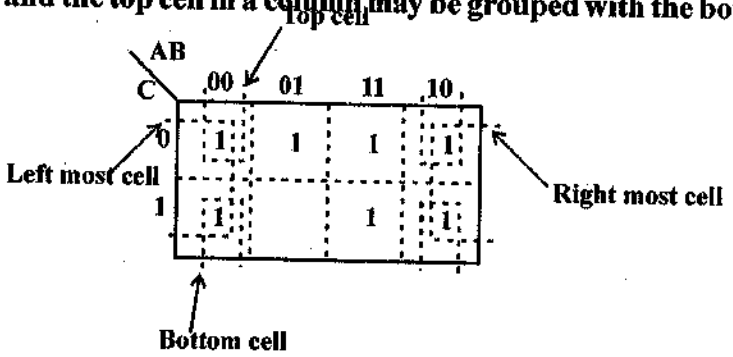


Figure:11.12

- **There should be as few groups as possible, as long as this does not contradict any of the previous rules.**

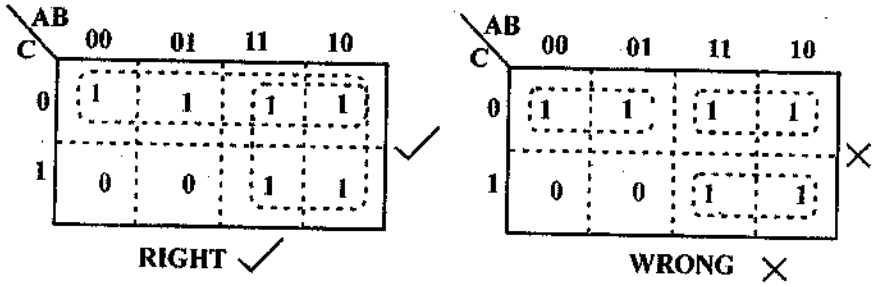


Figure:11.13

The number of adjacent squares that may be Grouped (Combined) must represent a number that is 2^n where n= 1,2,4. As the large number of adjacent squares is combined, we obtain a product term with fewer literals. In a four variable K-map:

1. One squares represent one minterm, giving a term of four literals.
2. Two adjacent squares represent a term of three literals. Thus combining two adjacent squares leads to eliminate one variable.
3. Four adjacent squares represent a term of two literals. i.e. Combining of four squares leads to eliminate two variables.
4. Eight adjacent squares represent a term of one literal. i.e. Combining of eight squares leads to eliminate three variables.
5. Sixteen adjacent squares represent the function equal to 1. Thus grouping of sixteen squares leads to eliminate all the four variables and the function is equal to 1.

Ex.–4. Simplify the Boolean expression given below using K-map technique

$F = \bar{A}BCD + A\bar{B}CD + AB\bar{C}D + ABC\bar{D}$

Solution: The expression for the function F contains four variables and thus can be mapped into a four variable K-map (2^4=16 of squares) as shown in Figure (11.14).

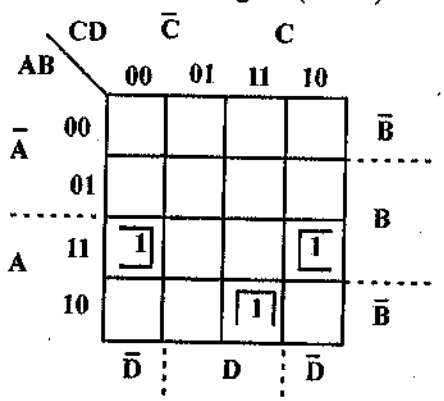


Figure: 11.14

The left and right columns are adjacent to each other and thus the terms $AB\bar{C}\bar{D}$ and $ABC\bar{D}$ can be combined to yield the single term $AB\bar{D}$. Likewise, the top and bottom rows are adjacent to each other and thus the terms $\bar{A}\bar{B}CD$ and $A\bar{B}CD$ can be combined to yield the single term $\bar{B}CD$. Therefore, the given expression can be written in simplified form as

$$F=AB\bar{D}+\bar{B}CD$$

Ex.–5. Simplify the Boolean function $F(x,y,z) = \sum(2,3,4,5)$

Solution: For the simplification of the above function a three variable K-map is required.

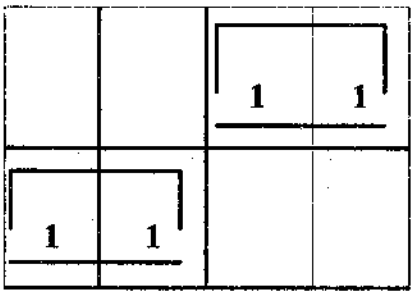


Figure: 11.15

In the K-map shown above, first, each minterm m_2= 010, m_3=011, m_4=100, and m_5=101 are marked with 1's. In the next step the possible adjacent squares are found and they are marked with in the map by two rectangles, each two 1's. The upper grouping gives the term AB and the lower one gives the AB. Thus

$$F=\bar{A}B+A\bar{B}$$

Ex.–6. Simplify the Boolean function $F(w,x,y,z)= \sum(0, 4, 9, 10, 14, 15)$

Solution: For the simplification of the above function a four variable K-map is required.

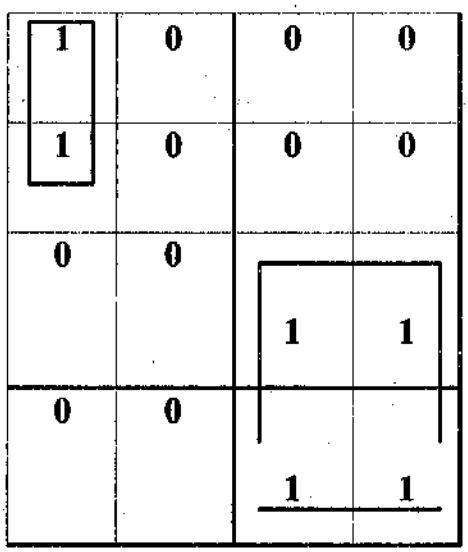


Figure: 11.16

$$F=\bar{W}\bar{Y}\bar{Z}+WY$$

11.12 DON'T CARE CONDITIONS

Quite often, we do not care if a variable represents a logical 1 or a logical 0. In this case it is convenient to represent that variable as a don't care. Don't care conditions allow us to obtain simpler Boolean expressions. Thus don't care" conditions is a sets of inputs for which the designer doesn't care what the output is. They are usually indicated on the map with a dash or X.

In other words the don't care condition means that a combination of input states do occur and whether the outputs for those states taken as 1's or 0's, it does not matter.

11.13 MINIMIZATION

The process of minimization using k-map technique and don't care condition can be illustrated in the following example.

Ex.–7. Simplify the Boolean function

$$F(w, x, y, z) = \sum(1,3,7,11,15)$$

that has the don't care conditions

$$d(w, x, y, z) = \sum(0, 2, 5)$$

Solution: For the simplification of the above function, four variable K-maps are drawn. In the two K-maps given below the minterms of F are marked with 1's and the do not care conditions d are marked with ×' s and the remaining are marked with 0' s.

For simplification of the function F as sum of products we have to include all the five 1's in the map but the choice of taking × as 0 or 1 and its inclusion depends upon the way of solving the function. The above function can be solved in two different ways shown below.

The final results are different but both of them satisfy the above conditions.

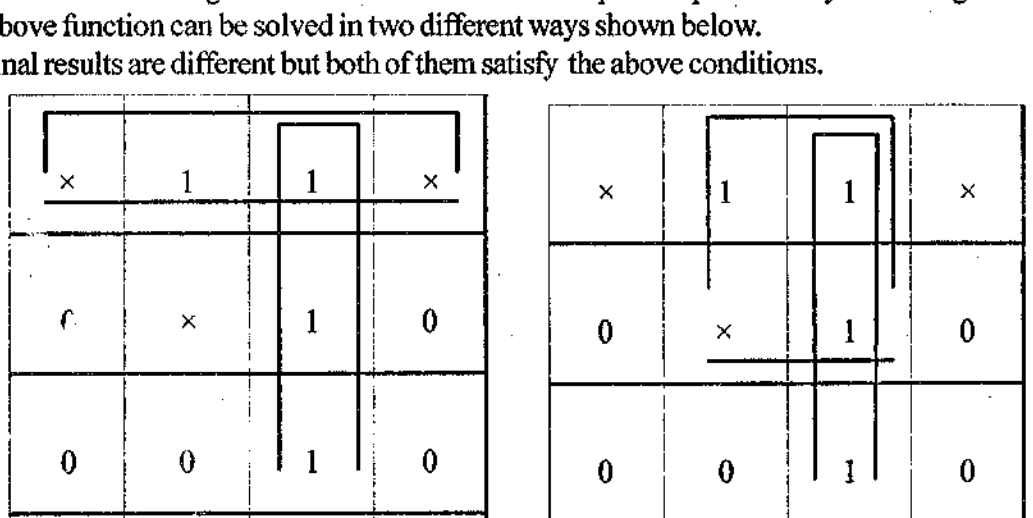


Figure: 11.17

The above k-map gives $F = yz + \bar{w}\,\bar{x}$ **This K-map gives** $F = yz + \bar{w}\,z$

Ex.–8. Simplify the Boolean function

$$F(w,x,y,z) = \sum(3,5,7,11,15)$$

that has the don't care conditions

$$d(w,x,y,z) = \sum(1,4,6)$$

Solution:

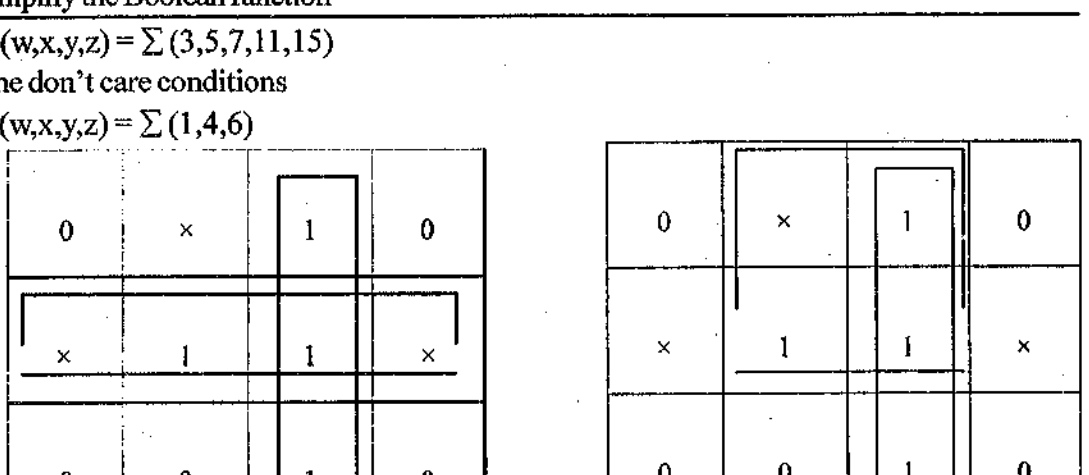


Figure: 11.18

The above k-map gives $F = yz + \bar{w}x$ The above k-map gives $F = yz + \bar{w}z$

The above function has been simplified in two different ways and the final results as sum of products are different but both of these simplified outputs satisfy the above conditions.

11.14 REVIEW QUESTIONS

Q.1. Describe the basic laws and properties of Boolean algebra.

Q.2. State and prove the De -Morgan's Theorems.

Q.3. Define the terms "minterm" and "maxterm" in Boolean algebra.

Q.4. Discuss the utilities of K-map technique.

Q.5. What do you mean by don't care condition.

Q.6. Simplify the Boolean function $F(w,x,y,z) = \sum(0,1,3,4,9,10,14,15)$.

Q.7. Simplify the Boolean function $F(w,x,y,z) = \sum(0,1,2,4,5,9,10,11,14,15)$.

Q.8. Simplify the Boolean function

$$F(w,x,y,z) = \sum(1,3,5,7,11,15)$$

that has the don't care conditions

$$d(w,x,y,z) = \sum(0,4,6)$$

Unit-12
ARITHMETIC CIRCUITS

Content of the Unit

12.0 OBJECTIVE

In this chapter we will discuss –

- Binary arithmetic is a combinatorial problem.
- The circuits for binary arithmetic can be designed using basic gates and their complex combina tions.
- The output of arithmetic circuit at any time depends upon the combination of the input signals present at that instant of time only.
- For the design of a digital system a thorough knowledge of the basics and applications binary arithmetic is essentials.
- This chapter presents an overview on the basics of binary arithmetic and its use in the design of adder and subtractor circuits.

12.1 INTRODUCTION

One of the basic arithmetic operations in digital electronics is the addition and subtraction of binary numbers. The simplest one is addition of two binary digits.

In two digit addition there are four possible elementary operations.

1. 0. + 0 = 0
2. 0 + 1 = 1
3. 1 + 0 = 1
4. 1 + 1 = 10

The first three operations produces a sum in terms of one digit but when both the inputs are 1, the binary sum is consists of two digits. The LSB (least significant bit) of the result t is called the SUM and MSB (most significant bit) is called carry. When the added numbers contains more significant digits, the carry obtained from addition of two bits is added to the next higher order pair of significant bits.

12.2 ADDERS

Binary adders are used to add binary numbers. Adder circuits take two binary numbers as input and add one binary number input to the other binary number input. Adders give out two outputs, SUM and Carry. There are two types of adders: Half adders and Full adders. A full adder is a logical circuit that performs an addition operation on three binary digits. A half adder is a logical circuit that performs an addition operation on two binary digits. A full adder is a logical circuit that performs an addition operation on three binary digits. The adder produces a sum and carries value, which are both binary digits.

12.2.1 Half-Adder

A *half-adder* is an arithmetic digital circuit that can be used to add two bits. Such a circuit thus has two inputs that represent the two bits to be added and two outputs, with one producing the SUM output and the other producing the CARRY. Figure 2.1 shows the truth table of a half-adder, showing all possible input combinations and the corresponding outputs. The Boolean expressions for the SUM and CARRY outputs are given by the equations

$$\text{SUM} = A.\overline{B} + \overline{A}.B$$

$$\text{CARRY C} = A.B$$

Examination of these two expressions shows that there is no scope for further simplification. While the first one representing the SUM output is that of an EXOR gate, the second one representing the CARRY output is that of an AND gate.

Table 12.1: Truth table for a Half Adder

A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

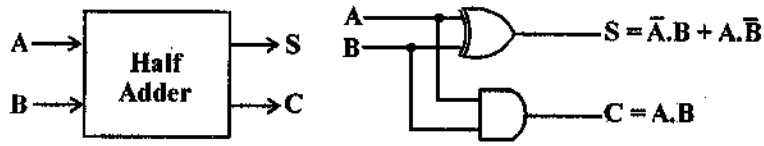


Figure 12.1: Circuit Symbol and logic diagram of a half-adder.

12.2.2 Full Adder

A *full adder* circuit is an arithmetic digital circuit that can be used to add three bits to produce a SUM and a CARRY output. Such a building block becomes a necessity when it comes to adding binary numbers with a large number of bits. The full adder circuit overcomes the limitation of the half-adder, which can be used to add two bits only. Since in the addition of LSBs of the two numbers, we record the sum under the LSB column and take the carry, if any, forward to the next higher column bits. As a result, when we add the next adjacent higher column bits, we would be required to add three bits if there were a carry from the previous addition. We have a similar situation for the other higher column bits also until we reach the MSB. A full adder is therefore essential for the hardware implementation of an adder circuit capable of adding larger binary numbers. A half-adder can be used for addition of LSBs only.

Figure 12.2: Symbolic diagram of a half-adder.

Table 12.2: Truth table for a Full adder

Inputs			Outputs	
A	B	C_{in}	C_{out} (Carry)	S (SUM)
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

In Table 12.2 the full adder truth table of a circuit showing all the possible input combinations and corresponding outputs. In order to arrive at the logic circuit for hardware implementation of a full adder, we will firstly write the Boolean expressions for the two output variables, that is, the SUM and CARRY outputs, in terms of input variables. These expressions are then simplified by using any of the simplification techniques described in the previous chapter. The Boolean expressions for the two output variables are given below.

$$S = \overline{A}.\overline{B}.C_{in} + \overline{A}.B.\overline{C}_{in} + A.\overline{B}.\overline{C}_{in} + A.B.C_{in}$$

$$C_{out} = \overline{A}.B.C_{in} + A.\overline{B}.C_{in} + A.B.\overline{C}_{in} + A.B.C_{in}$$

With the help of K-map method the expression for C_{out} can be simplified to

$$C_{out} = B.C_{in} + A.B. + A.C_{in}$$

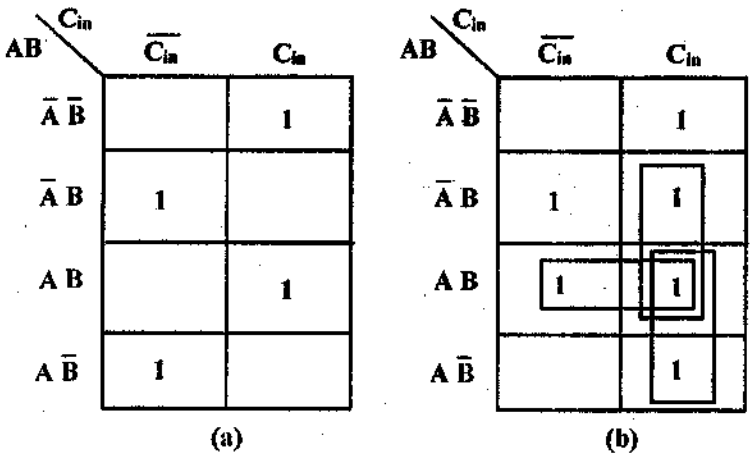


Figure 12.3: K-maps for the sum and carry-out of a full adder.

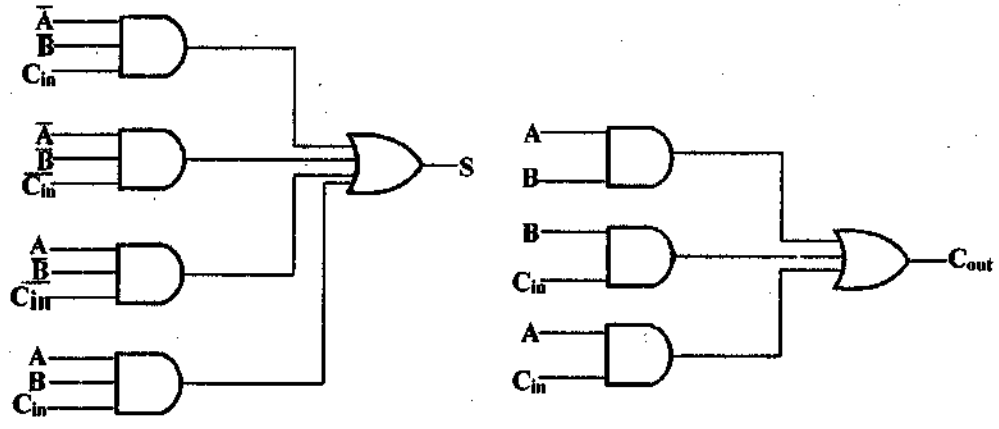


Figure 12.4: Logic circuit diagram of a full adder.

Figure (12.4) shows the logic circuit diagram of the full adder. A full adder can also be seen to comprise two half-adders and an OR gate. The expressions for SUM and CARRY outputs can be rewritten as follows:

$$S = \overline{C}_{in}.(\overline{A}.B + A.\overline{B}) + C_{in}.(A.B + \overline{A}.\overline{B})$$

$$S = \overline{C}_{in}.(\overline{A}.B + A.\overline{B}) + C_{in}.\overline{(\overline{A}.B + A.\overline{B})}$$

Similarly, the expression for CARRY output can be rewritten as follows:

$$C_{out} = B.C_{in}.(A + \overline{A}) + A.B + A.C_{in}.(B + \overline{B})$$

$$= A.B + A.B.C_{in} + \overline{A}.B.C_{in} + A.B.C_{in} + A.\overline{B}.C_{in}$$

$$= A.B + A.B.C_{in} + \overline{A}.B.C_{in}$$

$$= A.B(1 + C_{in}) + C_{in}.(\overline{A}.B + A.\overline{B})$$

$$C_{out} = A.B + C_{in}.(\overline{A}.B + A.\overline{B})$$

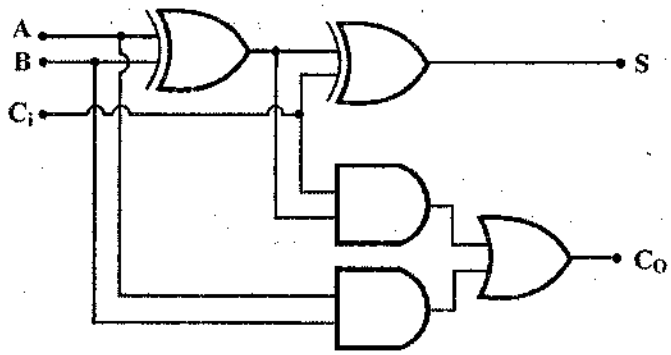


Figure 12.5 Logic implementation of a full adder.

Above Boolean expression can be implemented with a two-input EXOR gate provided that one of the inputs is C_{in} and the other input is the output of another two-input EXOR gate with A and B as its inputs. Similarly, the other Boolean expression can be implemented by OR ing two minterms. One of them is the AND output of A and B. The other is also the output of an AND gate whose inputs are C_{in} and the output of an EXOR operation on A and B. The whole idea of writing the Boolean expressions in this modified form was to demonstrate the use of a half-adder circuit in building a full adder. Figure (12.5 a) and (b) shows logic implementation of above Boolean equations.

Rearranging the circuit, it can be seen that it comprises two half-adders and an OR gate:

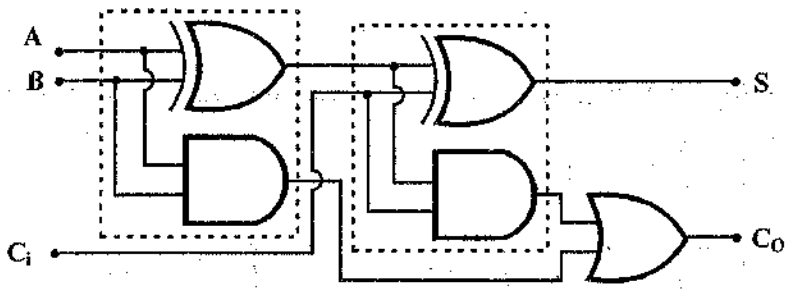


Figure 12.6: Logic implementation of a full adder using two half adders.

12.2.3 Parallel Binary adders

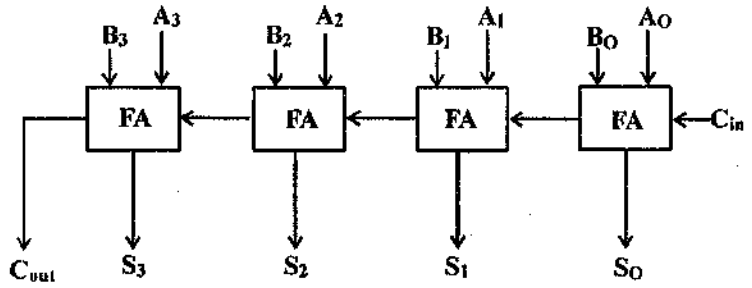


Figure 12.7: Circuit diagram of a 4-bit binary parallel adder.

The full adder of the type described in the last section is the basic building block of parallel binary adders. However, a single full adder circuit can be used to add one-bit binary numbers only. A cascade arrangement of these adders can be used to construct adders capable of adding binary numbers with a larger number of bits. For example, a four-bit binary adder would require four full adders of the type shown in Figure 12.4 to be connected in cascade. Figure 12.7 shows such an arrangement. $(A_3A_2A_1A)$ and $(B_3B_2B_1B_0)$ are the two binary numbers to be added, with A_0 and B_0 representing LSBs and A_3 and B_3 representing MSBs of the two 4-bit numbers.

The operation of the parallel adder can be understood with the help of the following example. Let $A_3A_2A_1A$ =1101 and $B_3B_2B_1B_0$ = 1011. These two 4-bit numbers can be added as

1101
1011

SUM =11000

In the circuit the two 4-bit binary number A and B are fed and the resultant Sum output will be shown as $C_{out}S_3S_2S_1S_0$.

12.2.4 BCD Adders

Binary coded decimal (BCD) addition is the same as binary addition with a bit of variation. In BCD Adders, whenever a sum is greater than 1001, it is not a valid BCD number, so we have to add 0110 to it, to do the correction. This will produce a carry, which is added to the next BCD position. For the BCD addition in first step the adding of the two 4-bit BCD code inputs will do. In the second step determine if the sum of this addition is greater than 1001; if yes, then add 0110 to this sum and generate a carry to the next decimal position. A BCD adder illustrating the addition *7 + 6 = 13* (0111 + 0110 = 0001 0011BCD) is shown below.

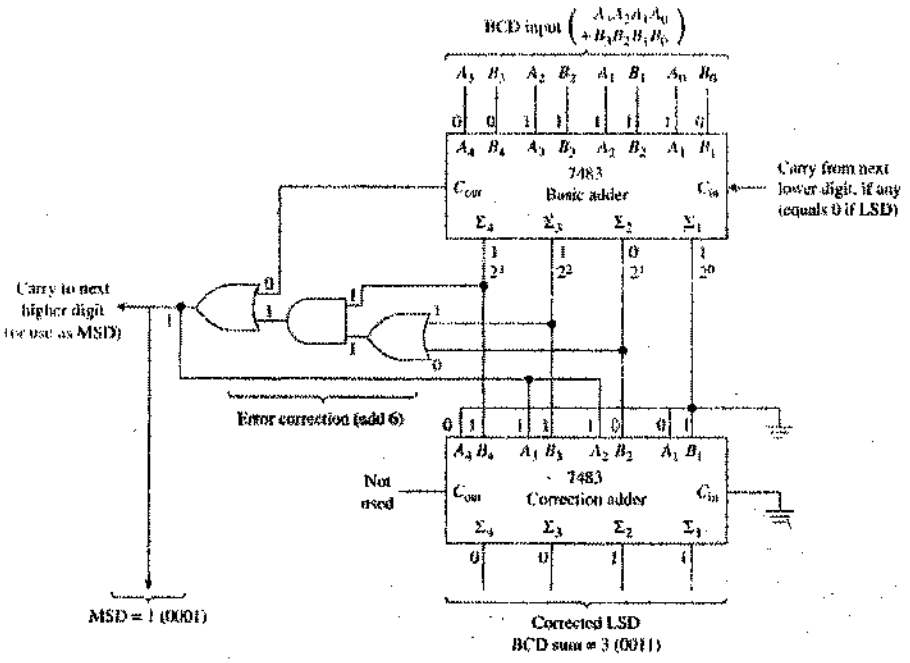


Figure 12.8: Circuit diagram of BCD adder.

12.2.5 2's Complement Adder

2's Complement

The **2's complement** of a **binary number** is defined as the value obtained by subtracting the number from a large power of two (specifically, from 2^N for an N-bit two's complement). The 2's complement of the number then behaves like the negative of the original number in most arithmetic, and it can coexist with positive numbers in a natural way.

Determination of the 2's Complement of a binary number

Take the One's complement of the binary number and add 1.

Examples

1. 10110 => 01001+1 = 01010
2. $(010011)_2$ can be converted into its 2's compliment using the following steps.

NOT(010011) = 101100 (Invert bits)

101100 + 000001 = 101101 (Add 1)

2's compliment of $(010011)_2$ = 101101

2's Compliment addition

2's complement addition follows the same rules as **binary addition.**

For example,

6+(–4) = 2 can be done using 2' compliment binary addition

In binary 6 =110, 4 = 100 and 2's compliment of 4 *i.e.* –4 = 011 + 001 = 100

So that $6 + (-4) = +2_{10} = 0110 + 1100 = 0010 = 2_{10}$

The circuit diagram of a 2's compliment binary adder is shown in figure.

The circuit will add the two numbers if one of the input of the entire four XOR gate is 0. Then the XOR gate will give the output equal to 1 if the input B is 1 or give 0 if input B is at 0. After that these B outputs are fed to the inputs of the full adders along with the A inputs. Rest of the function is same as of 4-bit full adder, which has been already explained in the last section.

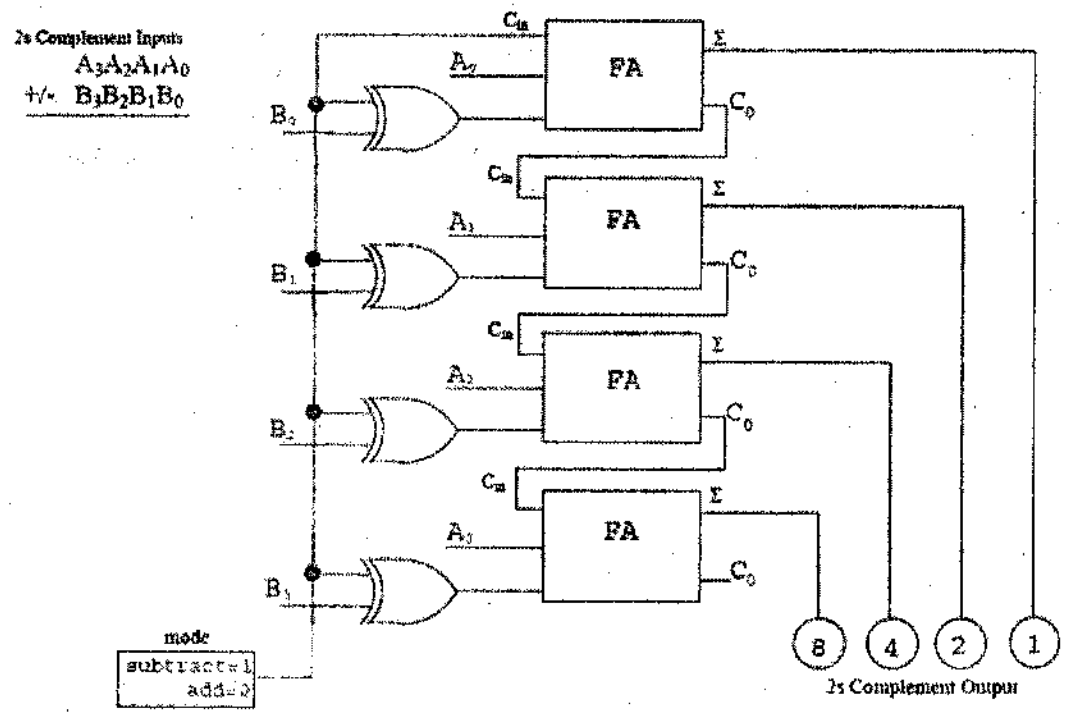


Figure 12.9: Bit binary adder designed using 2' compliment method

12.3 SUBTRACTORS

Subtractor circuits take two binary numbers as input and subtract one binary number input from the other binary number input. Similar to adders, it gives out two outputs, difference and borrows (carry-in the case of Adder). There are two types of subtractors.

- Half Subtractor.
- Full Subtractor.

12.3.1 Half Subtractor

The half-subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, X (minuend) and Y (subtrahend) and two outputs D (difference) and B (borrow). The symbolic, logic circuit diagram and truth table of a half subtractor are shown below. The Boolean expression for a two bit half subtractor are given as

Difference $D = \overline{A}.B + A.\overline{B}$

and Borrow $B_0 = \overline{A}.B$

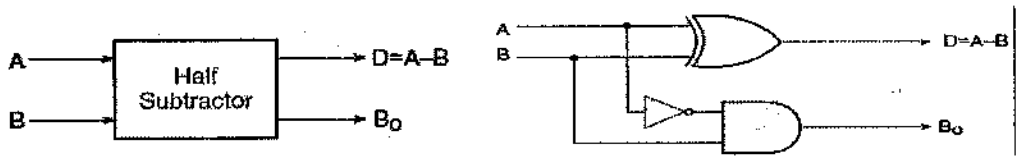


Figure 12.10: Circuit Symbol and logic diagram of a Half- Subtractor circuit

Table 12.3 Truth table of Half-Subtractor

A	B	B_o	D
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

12.3.2 Full Subtracter

A full subtracter is a combinational circuit that performs subtraction involving three bits, namely minuend, subtrahend, and borrow-in. Thus in the subtraction operation over two bits, a minuend and a subtrahend, and another bit is taken into consideration whether a '1' has already been borrowed by the previous adjacent lower minuend bitor not. As a result, there are three bits to be handled at the input of a full subtractor, namely the two bits to be subtracted and a borrow bit designated as Bin. There are two outputs, namely the DIFFERENCE output D and the BORROW output Bo. The BORROW output bit tells whether the minuend bit needs to borrow a '1' from the next possible higher minuend bit. The logic symbol and truth table are shown below. The Boolean expressions for the two output variables are given by the two equations given below.

$$D = \overline{A}.\overline{B}.B_{in} + \overline{A}.B.\overline{B}_{in} + A.\overline{B}.\overline{B}_{in} + A.B.B_{in}$$

$$B_0 = \overline{A}.\overline{B}.B_{in} + \overline{A}.B.\overline{B}_{in} + \overline{A}.B.B_{in} + A.B.B_{in}$$

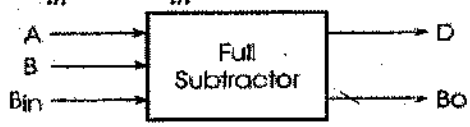
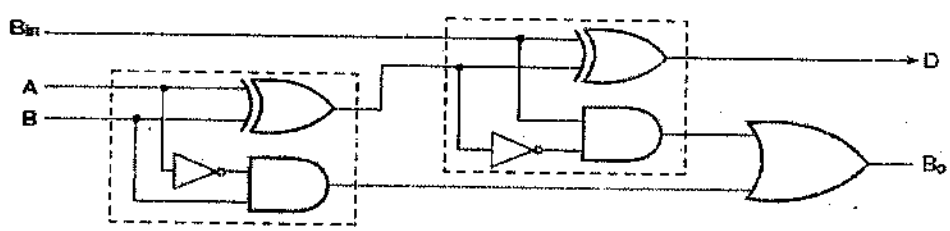


Figure 12.11: Circuit Symbol of a Full Subtractor circuit

Table 12.4 Truth table for a Full-Subtractor

Inputs			Outputs	
Minuend A	Subtrahend B	Borrow in B_{in}		

	Difference D	Borrow out B_o
0	0	0
	0	0
	0	0
	0	0
0	0	0
	1	0
	1	0
	1	0
0	1	0
	0	0
	1	0
	1	0
0	1	0
	1	0
	0	0
	1	0
	0	0
	0	0
	1	0
	1	0
	0	0
	0	0
	0	0
	1	0
	1	0
	1	0
	1	0



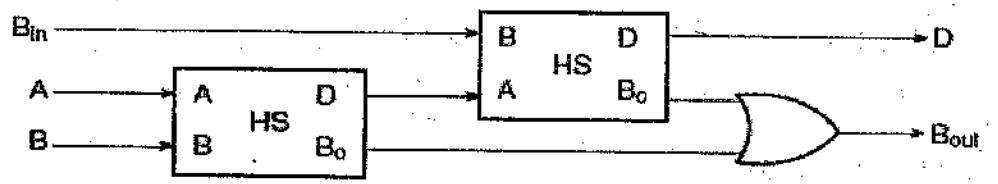


Figure 12.12 Logic implementation of a full subtractor using two half-subtractors.

12.3.3 Parallel Binary Subtractors

A parallel binary subtractor can be designed using 2's compliment subtraction method.

Subtraction of Binary Numbers using 2's Complement Method

1. Take the 2's complement of the subtrahend (bottom number).
2. Add the 2's complement to the minuend (top number)
3. Overflow indicates that the answer is positive. No end-around carry (EAC).
4. If there is no overflow then the answer is negative. Take the2's complement of the original sum to obtain the true magnitude of the answer.

Example (a) $19_{10} - 18_{10} = 1$ can be done in binary as:

$$\begin{array}{rr} 10011 & 10011 \\ -10010 & +01110 \\ & = 1\ 00001 \end{array}$$ (1 overflow indicates positive number)

(b) $18_{10} - 20_{10} = 2$ can be performed as

$$\begin{array}{rr} 10010 & 10010 \\ -10100 & +01100 \\ & = 11110 \end{array}$$

In this case there is no overflow therefore the answer is negative. So that we have to take the 2's complement of the original sum to obtain the true magnitude of the answer.

2's compliment of $11110 = 00001 + 00001 = 00010$

Ans $= -00010 = -2_{10}$.

2's compliment Subtractor

The circuit diagram of a / 4-bit parallel binary adder designed using the 2's compliment binary subtraction method is shown below.

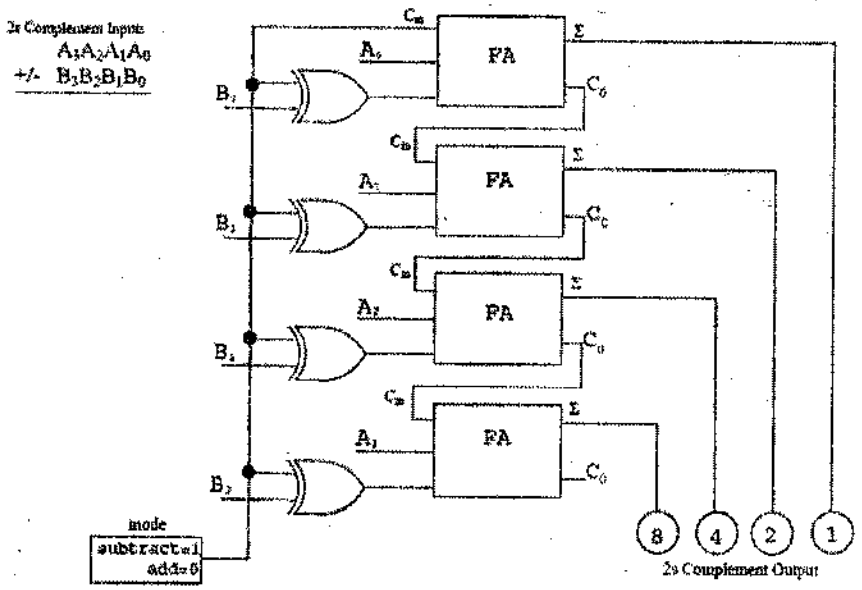


Figure 12.13: 4-bit Parallel binary subtractor designed using 2's compliment binary subtraction method

The circuit will subtract the two numbers if one of the inputs of the entire four XOR gate is 0. Then the XOR gate will give the output equal to 1 if the input B is 0 or give 1 if input B is at 0. Thus the XOR gate will give output equal to the compliment of B. Then these complimented B outputs are fed to the inputs of the full adders along with the A inputs. Rest of the function is same as of 4-bit full adder, which

has been already explained in the last section. In the final sum a number 0001 is added. Then if an end-around carry is generated then the answer is the final sum and a positive number. Otherwise if there is no overflow then the answer is negative and for that take the 2's complement of the original sum with negative sign is the answer.

12.4 COMPARATOR

A comparator is a device which compares two inputs (voltages or currents) and switches its output to indicate which one is larger. The simplest comparator is the OP_AMP difference amplifier. The circuit given below compares the two signals V_1 and V_2 and gives the output as

$V_{out} = A(V_1 - V_2)$, where A is the gain of the amplifier.

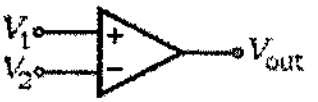


Figure 12.15 Circuit of a simple op-amp comparator.

12.5 REVIEW QUESTIONS

Q.1. What do you mean by binary addition? Draw the circuit of binary half-adder and explain its operation.

Q.2. What do you mean by binary subtraction? Draw the circuit of binary half-subtractor and ex plain its operation.

Q.3. Determine the 2's compliment of the binary number $(01001101)_2$.

Q.4. Draw the circuit of Full-adder and explain its operation and also show that it can be designed using two half-adders.

Q.5. Draw the circuit of Full-Subtractor and explain its operation and also show that it can be designed using two half-subtractors.

Q.6. Explain the operation of 4-bit binary parallel adder.

Q.7. Describe the functioning of a 4-bit binary parallel subtractor.

Q.8. Explain the methodology of binary subtraction using 2's compliment.

Unit-13
COMBINATIONAL CIRCUITS

Content of the Unit

13.0 OBJECTIVE

In this chapter we will discuss –

- Combinational circuits are the basic building blocks of complex digital system.
- This chapter presents a class of building blocks that can be used to design complex combina tional circuits, and covers building blocks such as multiplexers and de-multiplexers and other derived devices such as encoders and decoders.
- Emphasis is given to the operational basics and use of these devices to design more complex combinational circuits.

13.1 INTRODUCTION

Combinational circuits are designed using basic gates and their complex combinations. The output of a combinational circuit at any time depends upon the combination of the input signals present at that instant of time only, and does not depends upon any past state or conditions. For the design of a digital system a thorough knowledge of the basics and applications of combinational circuits is essentials.

13.2 MULTIPLEXER

The term 'Multiplex' means "many into one". A multiplexer is a combinatorial circuit that is given a certain number (usually a power of two) *data inputs*, let us say 2^n, and n *address inputs* used as a binary number to select one of the data inputs. The multiplexer has a single output, which has the same value as the selected data input. Thus Multiplexer performs multiplexing; it selects one of many analog or digital input signals and forwards the selected input into a single line. A multiplexer or MUX, also called a data selector, is a combinational circuit with more than one input line, one output line and more than one selection line. A multiplexer of 2^n inputs has n select lines, which are used to select which input line to send to the output. Figure 13.1 depicts the symbolic diagram of a 4-to-1 line MUX. There are four inputs (I_0, I_1, I2 and I_3), two select lines (X_1 and X_0) and one output at Y.

Data Select inputs		Output
X_1	X_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

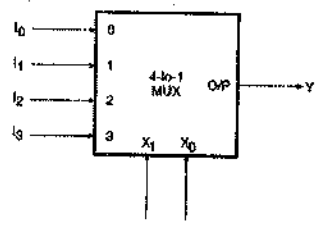


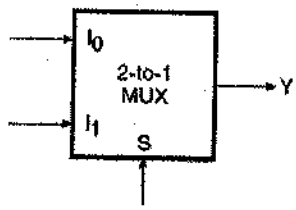
Figure 13.1. Block diagram and functional table of a 4-to-1 multiplexer

Now we will briefly describe the type of combinational logic circuit found inside a multiplexer by considering the 2-to-1 multiplexer in Fig. 13.2(a), the functional table of which is shown in Fig. 13.2(b) and the possible circuit diagram is shown in Figure 13.2(c) Operation of this circuit is govern by following Boolean function

$Y = I_0\bar{S} + I_1S$

- For $S = 0$, the Boolean expression for the output becomes $Y = I_0$.
- For $S = 1$, the Boolean expression for the output becomes $Y = I_1$.

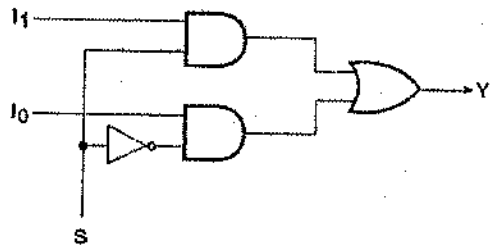
Thus, inputs I_0 and I_1 are respectively switched to the output for $S = 0$ and $S = 1$.



(a)

S	Y
0	I_0
1	I_1

(b)



(c)

Figure 13.2. (a) 2-to-1 multiplexer circuit representation, (b) 2-to-1 multiplexer truth table and (c) 2-to-1 multiplexer.

Similarly a 4–to–1 multiplexer can be designed. Two selection lines are required for the select of 4 lines to one output. The input combinations are 00, 01, 10 and 11 on the select lines respectively switch I_0, I_1, I_2 and I_3 to the output. The operation of the circuit is governed by the Boolean function.

$$Y = I_{00\ 1} + I_1S_{0\ 1} + I_{20}S_1 + I_3S_1S_0$$

Applications of *Multiplexers*

Multiplexers can be used as data selector as well as Parallel-to-Serial Data Conversion. Since data are processed in parallel in many digital systems to achieve faster processing speeds, when it comes to transmitting these data relatively large distances, this is done serially. The parallel arrangement in this case is highly undesirable as it would require a large number of transmission lines. Multiplexers can possibly be used for parallel-to-serial conversion. Figure 13.3 shows one such arrangement where a 4-to-1 multiplexer is used to convert four-bit parallel binary data to serial form. A two -bit counter controls the selection inputs. As the counter goes through 00 to 11, the multiplexer output goes through I_0 to I_3.

Select		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

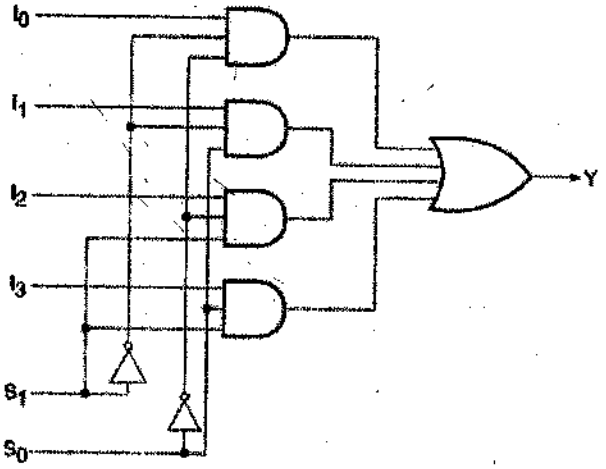


Figure 13.3. Logic diagram and truth table for a 4-to-1 multiplexer.

13.3 MULTIPLEXER TREE

When large number of input available then the MUX can be designed using two or more MUX and the resultant circuit is known as Multiplexer Tree. A design of 16-to-1 line MUX is illustrated below. In the design two 8×1 MUX are used. The 16×1 MUX circuit functions in the following manner. When S_3 is in logic '0' state, the upper multiplexer is enabled and the lower multiplexer is disabled. If we remember the truth table of a four-variable Boolean function, S_3 would be '0' for the first eight entries and '1' for the remaining eight entries. Therefore, when $S_3 = 0$ the final output will be any of the inputs from D_0 to D_7, depending upon the logic status of S_2, S_1 and S_0. Similarly, when $S_3 = 1$ the final output will be any of the inputs from D_8 to D_{15}, again depending upon the logic status of S_2, S_1 and S_0. The circuit therefore implements the truth table of a 16×1 multiplexer.

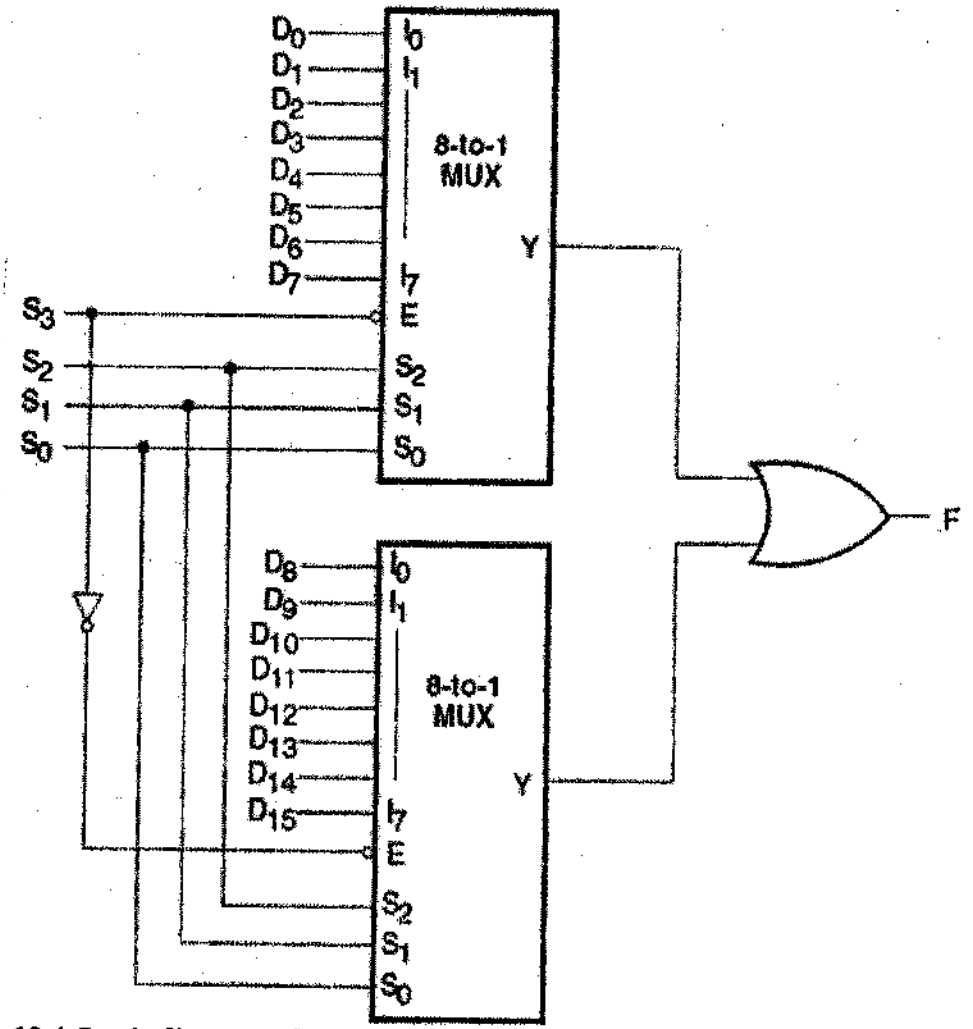
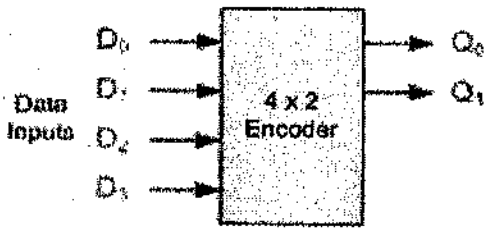


Figure 13.4: Logic diagram of a 16×1 multiplexer designed using two 8×1 multiplexers.

13.4 ENCODERS

An *encoder* is a multiplexer without its single output line. It is a combinational logic function that has 2^n (or fewer) input lines and n output lines, which correspond to n selection lines in a multiplexer. The n output lines generate the binary code for the possible 2^n input lines. A 4×2 encoder and its truth table are shown in Figure.



Inputs				Outputs	
D_3	D_2	D_1	D_0	Q_1	Q_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1
0	0	0	0	x	x

Figure 13.5: Block diagram and truth table for a 4×2 encoder.

The operation of an encoder can be understood with the following example. Let us take the case of an octal-to-binary encoder. Such an encoder would have eight input lines, each representing an octal digit, and three output lines representing the three-bit binary equivalent. The truth table of such an encoder is given in Table 13.1. In the truth table, the inputs D_0 to D_7 represent octal digits 0 to 7. The outputs A, B and C represent the binary digits. A possible circuit diagram for an octal to binary encoder is shown in Figure (13.4).

Table 13.1: Truth table of an encoder.

Inputs								Outputs		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	A	B	C
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

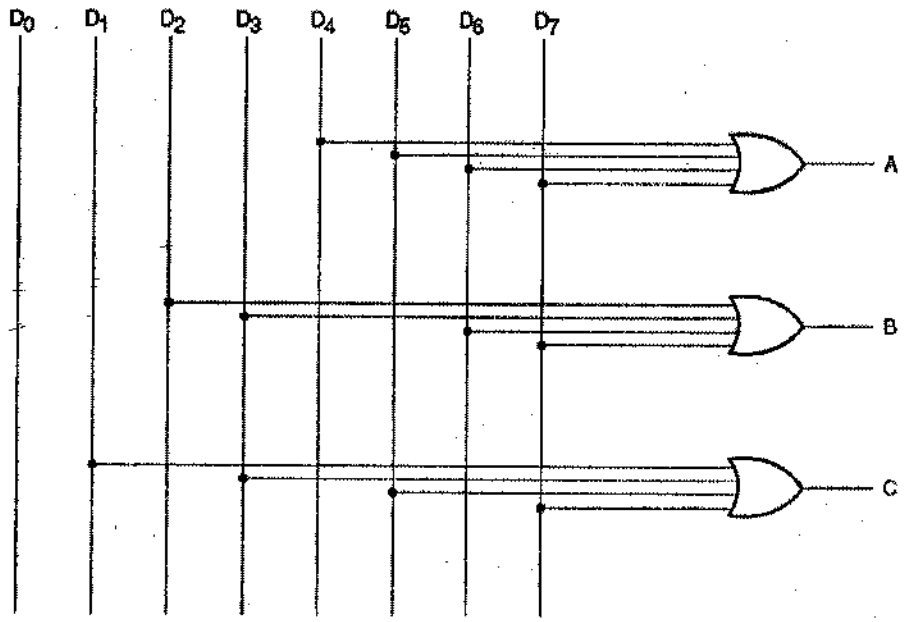
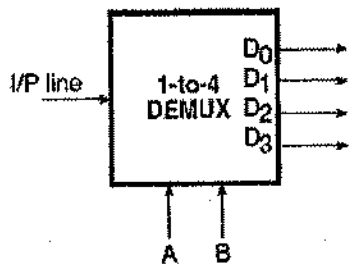


Figure 13.6. Logical circuit diagram of an 8×3 Encoder.

13.5 DEMULTIPLEXERS

The demultiplexer is the inverse of the multiplexer, in that it takes a single data input and n address inputs. The address input determine which data output is going to have the same value as the data input. The other data outputs will have the value 0. A *demultiplexer* is a combinational logic circuit with an input line, 2^n output lines and n select lines. It routes the information present on the input line to any of the output lines. The output line that gets the information present on the input line is decided by the bit status of the selection lines. Figure 13.5(a) shows the block diagram of a 1-to-4 demultiplexer. Figure 13.5(b) shows the truth table of the demultiplexer when the input line is held HIGH. The logical circuit diagram of a 1×4 demultiplexer is shown in Figure (13.8).

Inputs	Select		Outputs			
	A	B	D_0	D_1	D_2	D_3
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1



(a)

Figure 13.7: 1-to-4 demultiplexer.

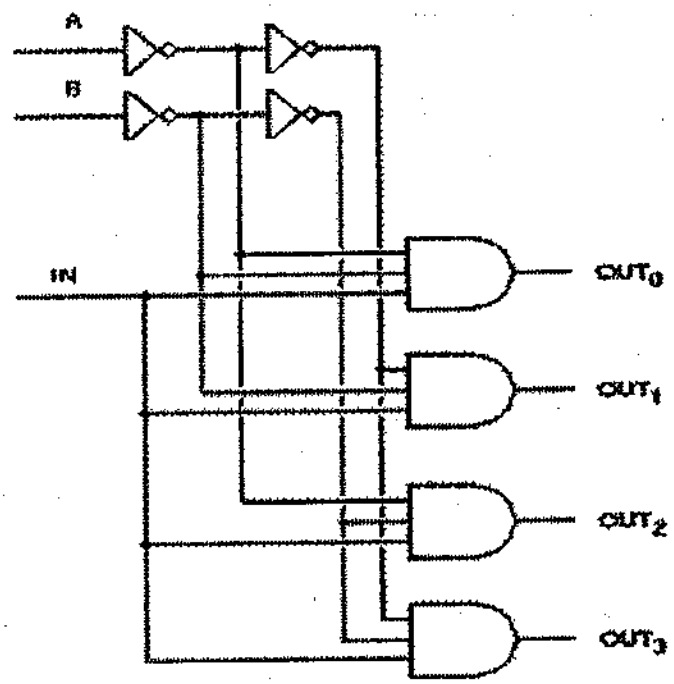


Figure 13.8: Logic diagram of a 1-to-4 demultiplexer

13.6 DEMULTIPLEXER TREE

When the requirement of a device that passes one set of two signals among four signals then a "two-bit1-to-2 demultiplexer" can be designed in the following manner.

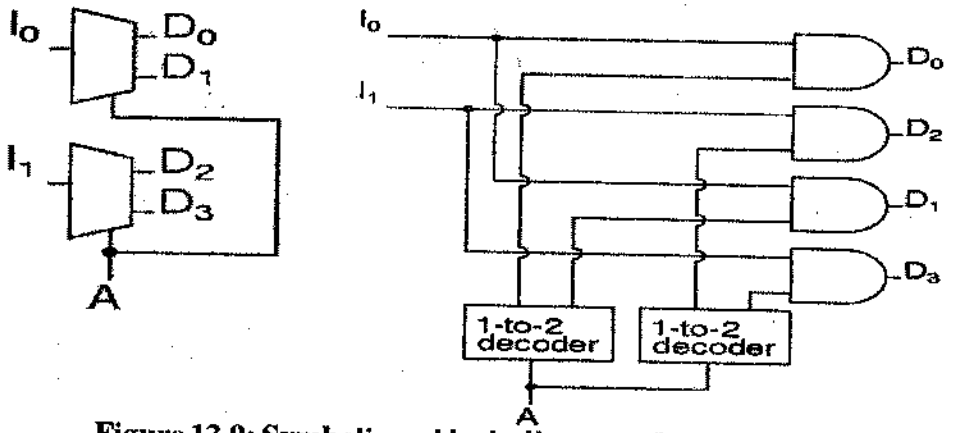


Figure 13.9: Symbolic and logic diagram of a demultiplexer tree (two bit 1-to-2 demultiplexer)

13.7 DECODERS

A *decoder* is a special case of a demultiplexer without the input line. Thus decoder is a combinational circuit that decodes the information on n input lines to a maximum of 2^n unique output lines. Figure 13.6 shows the circuit representation of 2-to-4 and 3-to-8 decoders. If there are some unused or 'don't care' combinations in the n-bit code, then there will be fewer than 2n output lines. For example, if there are three input lines, it can have a maximum of eight unique output lines. If, in the three-bit input code, the only used three-bit combinations are 000, 001, 010, 100, 110 and 111 (011 and 101 being either unused or don't care combinations), then this decoder will have only six output lines. In general, if n and m are respectively the numbers of input and output lines, then m d" 2n. A decoder can generate a maximum of 2^n possible minterms with an n-bit binary code.

In order explain the operation of a decoder; consider the logic circuit diagram in Fig. 13.10. This logic circuit, as we will see, implements a 3-to-8 line decoder function. This decoder has three inputs designated as A , B and C and eight outputs designated as D_0, D_1, D_2, D_3, D_4, D_5, D_6 and D_7. From the truth table given along with the logic diagram it is clear that, for any given input combination, only one of the eight outputs is in logic '1' state. Thus, each output produces a certain minterm that corresponds to the binary number currently present at the input. In the present case, D_0, D_1, D_2, D_3, D_4, D_5, D_6 and D_7 respectively represent the following minterms:

$D_{0\rightarrow}ABC$ $D_{1\rightarrow}AB\,C$ $D_{2\rightarrow}ABC$ $D_{3\rightarrow}\ ABC$

$D_{4\rightarrow}ABC$ $D_{5\rightarrow}\ ABCC$ $D_{6\rightarrow}\ ABC$ $D_{7\rightarrow}\ ABC$

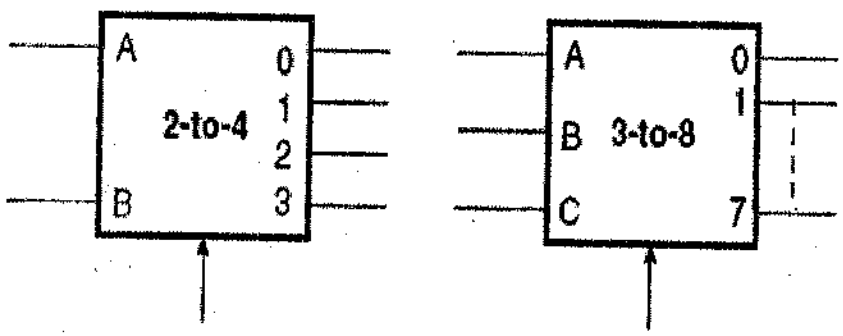


Figure 13.10. Block diagrams of 2-to-4 and 3-to-8 decoders.

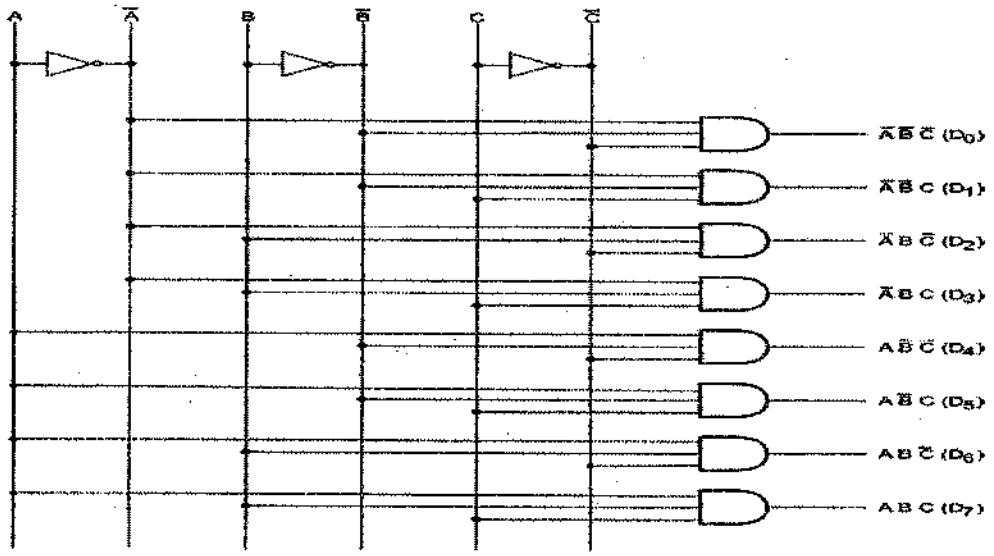


Figure 13.11: Logic diagram of 3 to-8 line decoder.

A typical design of a 3-to-8 line decoder is shown in the figure 13.9 and the table 13.2 presents the operation of the circuit. For a 3 input decoder maximum value of the possible out Puts can be 2^3=8.

Table 13.2: Truth Table for a 3 to 8 line decoder

Inputs			Outputs							
A	B	C	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

13.8 DIGITAL COMPARATOR

A digital comparator or magnitude comparator is a digital circuit that takes two numbers as input in **binary** form and compares whether one number is greater than, less than or equal to the other number. **Digital Comparators** can compare a variable or unknown number for example A (A1, A2, A3 ... An, etc) against that of a constant or known value such as B (B1, B2, B3 ... Bn, etc) and produce an output depending upon the result. For example, a comparator of 1-bit, (A and B) would produce the following three output conditions.

A < B, A = B and A > B

Inputs		Outputs		
A	B	A<B	A=B	A>B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

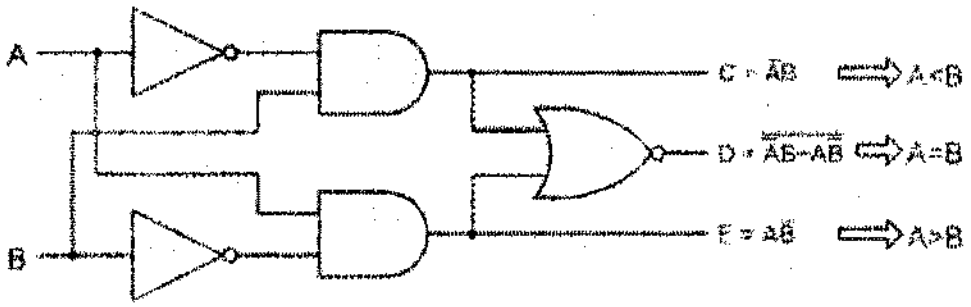


Figure 13.12: The logical circuit diagram and truth table of a 1-bit digital comparator.

13.9 PRIORITY ENCODERS

In digital electronics a priority encoder is a combinational circuit with $m = 2^n$ inputs and n outputs. Each of the m inputs is assigned a priority. The most significant bit of the input has the highest priority while the least significant bit has the lowest priority. The n bits of the output are the binary index of the non-zero input bit with highest priority, all input bits with lower priority will be ignored. For example, when n=2 and m=4 and, the behavior of the priority encoder can be described as the following truth table: where highest-priority inputs are to the left and "x" indicates either a 1 or a 0.

Inputs				Outputs	
A_3	A_2	A_1	A_0	F_1	F_0
0	0	0	x	0	0
0	0	1	x	0	1
0	1	x	x	1	0
1	x	x	x	1	1

A binary decoder can be used to convert the n-bit output of a priority encoder to a set of $m = 2^n$ bits each for one of the m devices.

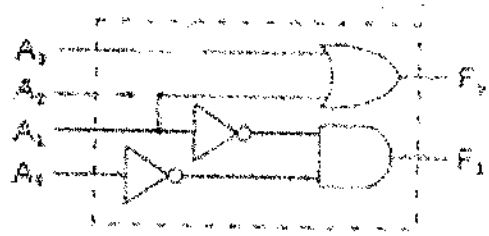


Figure 13.13: Logic diagram of a single bit 4-to-2 line priority encoder.

13.10 PARITY GENERATORS/CHECKERS

A parity generator is a circuit that, given an n-1 bit data word, generates an extra parity bit that is transmitted with the word. The value of this parity bit is determined by the bits of the data word. In an even parity scheme, the parity bit is a 1 if there is an odd number of 1's in the data word. Thus when we examine all the bits transmitted (data word + parity), we see an even number of one's (thus "even" parity). If the sum of the binary bits in word is odd (called odd parity).

In communications, parity checking refers to the use of parity bits to check that data has been transmitted accurately. The parity bit is added to every data unit (typically seven or eight bits) that is transmitted. The parity bit for each unit is set so that all bytes have either an odd number or an even number of set bits. At the receiving end of the transmission, a parity checker uses this extra information to detect single-bit errors in the transmitted data word.

It does so by regenerating the parity bit in the same manner as the generator and comparing the two parity bits. Disagreement between these bits means that one of the transmitted bits is incorrect, though the checker cannot determine which bit is in error. Note that single-bit parity scheme is unable to detect an even number of errors (e.g. 4 bits are wrong).

The output of a XOR gate is 1 if and only if one input is 1 and the other is 0. Alternatively stated, the output is 1 if the sum of the digits is 1. A circuit of a parity generator can be designed using this concept to the XOR tree.

Figure 13 shows that P=1 if the sum of D_0, D_1, D_2, and D_3 is odd. Hence, if the input P is grounded then P=0 for odd parity and P=1 for even parity. This figure can be used to generate parity bit E or check the parity bit P.

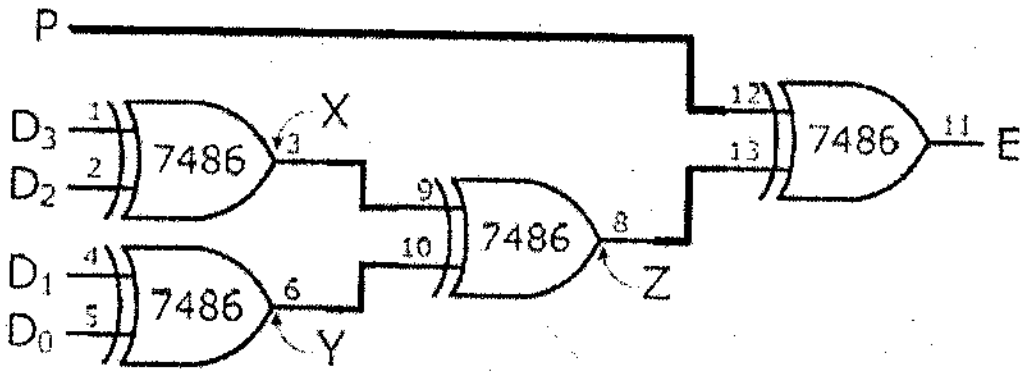


Figure 13.14: Parity –bit- generator/checker Circuit.

13.11 REVIEW QUESTIONS

Q.1. What is a multiplexer? Draw the circuit of a 2-to-1 line MUX and explain its operation.

Q.2. What do you mean by demultiplexer? Draw the circuit of a 1-to-4 line demultiplexer and explain its operation.

Q.3. Distinguish between decoder and demultiplexer.

Unit-14
SEQUENTIAL DIGITAL SYSTEMS

Content of the Unit

14.0 OBJECTIVE

In this chapter we will discuss –

- Registers and counters are the most important circuits in digital electronics.
- Using registers an information in bit form can be registered and stored.
- Counters are useful in counting the clock pulses. For the design of these circuits we need flip-flops.
- A flip-flop is the basic memory cell which can store 1-bit information.
- This Unit gives an overview of the flip-flops, registers and counters.

14.1 INTRODUCTION

In Combinational logic circuits the outputs at a given instant of time depend only upon the values of the input signals at the same moment. Such a system is said to have no memory. Sequential Logic circuits have some form of inherent "Memory" built in to them and they are able to take into account their previous input state as well as those actually present, a sort of "before" and "after" is involved. They are generally termed as two state or bi-stable devices which can have their output set in either of two basic states, a logic level "1" or a logic level "0" and will remain "latched" indefinitely in this current state or condition until some other input trigger pulse or signal is applied which will cause it to change its state once again. Registers, shift registers and counters are digital electronic devices that can be constructed using a clocked sequential circuit consists of group of flip-flops and combinational logic gates connected to form a feed path.

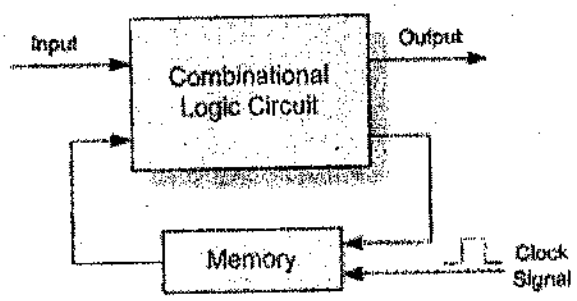


Figure 14.1: Block diagram of a Sequential circuit.

The word "Sequential" means that things happen in a "sequence", one after another and in **sequential logic** circuits, the actual clock signal determines when things will happen next. Simple sequential logic circuits can be constructed from standard bi-stable circuits such as Flip-flops, Latches and which themselves can be made by simply connecting together NAND/NOR Gates in a particular combinational way to produce the required sequential circuit. The block diagram of a sequential circuit is shown in figure. The system is consists of a combinational circuit to which a memory elements are connected to form a feedback path. The memory elements are devices capable of storing binary data. The sequential circuit receives binary data from external inputs and together with the present state of the memory data, determines the output.

14.2 FLIP-FLOP

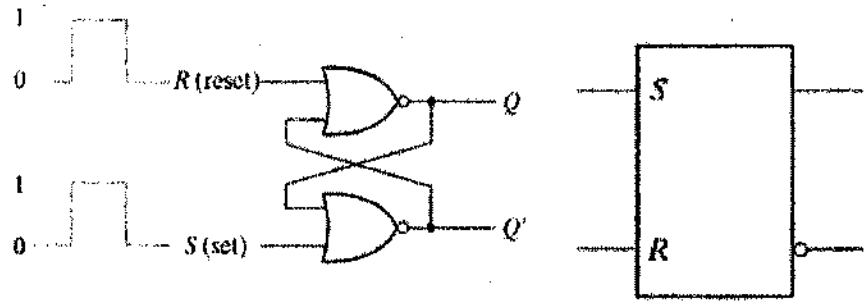
A flip-flop is a term referring to an electronic system that has two stable states and thereby is capable of serving as one bit of memory. A flip-flop is usually controlled by one or two control signals and/or a gate or clock signal. The output often includes the complement as well as the normal output. The term "Flip-flop" relates to the actual operation of the circuit, as it can be "Flipped" into one logic state or "Flopped" back into another.

14.2.1 A 1-bit Memory Storage Cell

The basic digital memory circuit which can be constructed by cross-coupling of two NOT gates. The output of each NOT gate is connected to the input of the other. This type of the feedback combination is called a FLIP-FLOP. The most important property of this circuit is that it can exist in one of the two stable states either Q=1 ($\bar{Q}$=0), called the 1 state, or Q=0(=1), referred to as the 0 state. This two stable state circuit is also known as a binary because it may store one bit of information (either Q=1 or Q=0), it is 1-bit memory cell or a 1-bit storage unit. Since this information is locked/latched and that is why the circuit is commonly known as a latch.

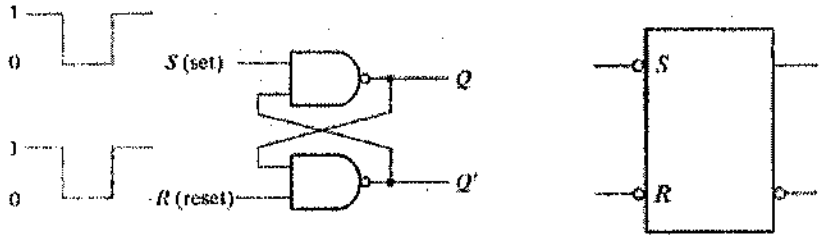
14.2.2 SR Flip-Flop

A **SR Flip-Flop** can be considered as a basic one-bit memory device that has two inputs, one which will "SET" the device and another which will "RESET" the device back to its original state, and an output Q that will be either at a logic level "1" or logic "0" depending upon this Set/Reset condition. The most fundamental latch is the simple *SR latch*, where S and R stand for *set* and *reset*. It can be constructed from a pair of cross-coupled NAND (or NOR) logic gates. A basic NAND/NOR Gate SR flip flop circuit provides feedback from its outputs to its inputs and is commonly used in memory circuits to store data bits. The simplest way to make any basic one-bit Set/Reset SR flip-flop is to connect together a pair of cross-coupled 2-input NAND Gates to form a SR NAND Gate Latch, so that there is feedback from each output to one of the other NAND Gate inputs. This device consists of two inputs, one called the Reset, R and the other called the Set, S with two corresponding outputs Q and its inverse or complement Q as shown below. The stored bit is present on the output marked Q. Generally, in the storage mode, the S and R inputs are both low, and feedback maintains the Q and outputs in a constant state, with the complement of Q. If S = 1 while R =0, then Q = 1, and Q stays to state 1 when S returns to S = 0; similarly, if R =1 and S = 0, then the output Q = 0, and Q stays to Q=0 when R returns to R = 0. The basic circuits of NAND and NOR latches along with their function table are shown below.



Inputs		Outputs		Function state
S	R	Q	$\overline{Q}$	
1	0	1	0	Set state
0	0	1	0	after S=1 and R=0
0	1	0	1	Reset state
0	0	0	1	after S=0 and R=1
1	1	0	0	Not allowed

Figure 14.2: Basic Flip-Flop circuit using NOR gates and its truth table.



Inputs		Outputs		Functional state
S	R	Q	$\overline{Q}$	
1	0	0	1	Set state
1	1	0	1	after S=1 and R=0
0	1	1	0	Reset state
1	1	1	0	after S=0 and R=1
0	0	1	1	Not allowed

Figure 14.3: Basic Flip-Flop circuit using NAND gates and its truth table.

Thus a flip-flop has two useful states. When Q=1 and = 0, it is the set state (or 1 state). When Q=0 and =1, it is the clear (reset) state (or o state). The outputs Q and are compliments of each other and are referred to as the normal and compliment outputs. Generally the binary state of the flip-flop is taken to be values of the normal output.

14.2.3 Clocked SR Flip-Flop

When latches are used for the memory elements in sequential circuits, a serious difficulty arises. Remember that latches have the property of immediate output responses. Because of this the output of a latch cannot be applied directly (or through logic) to the input of the same or another latch when all the latches are triggered by a common clock source. Flip-flops are used to overcome this difficulty. It is sometimes desirable in sequential logic circuits to have a bistable SR flip-flop that only change state when certain conditions are met regardless of the condition of either the Set or the Reset inputs. By connecting a 2-input NAND gate in series with each input terminal of the SR Flip-flop a Gated SR Flip-flop can be created. This extra conditional input is called an "Enable (clock)" input and is given the prefix of "C" as shown below.

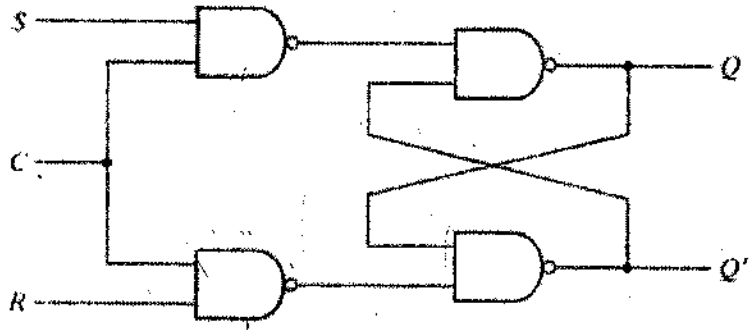


Figure 14.4: Symbolic and logic diagram of a SR Flip-Flop.

When the clock input "C" is at logic level "0", the outputs of the two AND gates are also at logic level "0", (AND Gate principles) regardless of the condition of the two inputs S and R, latching the two outputs Q and Q into their last known state. When the enable input "C" changes to logic level "1" the circuit responds as a normal SR bistable flip-flop with the two AND gates becoming transparent to the Set and Reset signals. This enable input can also be connected to a clock timing signal adding clock synchronization to the flip-flop creating what is sometimes called a "Clocked SR Flip-flop".

The Set State

Consider the circuit shown above. If the input R is at logic level "0" (R = 0) and input S is at logic level "1" (S = 1), a clock pulse is applied then the NAND Gate **Y** has at least one of its inputs at logic "0" therefore, its output Q must be at a logic level "1" (NAND Gate principles). Output Q is also fed back to input A and so both inputs to the NAND Gate **X** are at logic level "1", and therefore its output Q must be at logic level "0". Again NAND gate principals. If the Reset input R changes state, and now becomes logic "1" with S remaining HIGH at logic level "1", NAND Gate **Y** inputs are now R = "1" and B = "0" and since one of its inputs is still at logic level "0" the output at Q remains at logic level "1" and the circuit is said to be "Latched" or "Set" with Q = "1" and Q = "0".

The Reset State

In this second stable state, Q is at logic level "0", Q = "0" its inverse output is at logic level "1", not Q = "1", and is given by R = "1" and S = "0". As gate **X** has one of its inputs at logic "0" its output Q must equal logic level "1" (again NAND gate principles). Output Q is fed back to input B, so both inputs to NAND gate Y are at logic "1", therefore, Q = "0". If the set input, S now changes state to logic "1" with R remaining at logic "1", output Q still remains LOW at logic level "0" and the circuit's "Reset" state has been latched.

The Indeterminate or Undefined/ambiguous State

Table 14.1: Truth Table of a Clocked SR flip-flop

Inputs			Output	Operation mode
Q_n	S	R	Q_{n+1}	
0	0	0	Q_n	No Change state
0	1	0	1	Set
1	0	0	1	No Change state after S=1 and R=0
1	0	1	0	Reset state
0	0	0	0	No Change state after S=0 and R=1
0	1	1	?	Forbidden state

It is observed that when both inputs S = "1" and R = "1" the outputs Q and can be at either logic level "1" or "0", depending upon the state of inputs S or R BEFORE this input condition existed. However, input state R = "0" and S = "0" is an undesirable or invalid condition and must be avoided

because this will give both outputs Q and to be at logic level "1" at the same time and we would normally want Q to be the inverse of. However, if the two inputs are now switched HIGH again after this condition to logic "1", both the outputs will go LOW resulting in the flip-flop becoming unstable and switch to an unknown data state based upon the unbalance. This unbalance can cause one of the outputs to switch faster than the other resulting in the flip-flop switching to one state or the other which may not be the required state and data corruption will exist. This unstable condition is known as its **Meta-stable** state. Then, a bistable latch is activated or Set by a logic "1" applied to its S input and deactivated or Reset by a logic "1" applied to its R. The SR Latch is said to be in an "invalid" condition (Meta-stable) if both the Set and Reset inputs are activated simultaneously. In order to get rid of this problem a new type of flip-flop is required, which can remove this ambiguity.

14.2.4 JK Flip-Flop

From the last section we know that the basic clocked SR Flip-flop suffers from two basic problems: First one occurs when S = 1 and R = 1 condition or S = R = 1 must always be avoided. The second one, if S or R change state while the enable input is high the correct latching action will not occur. Then to overcome these two problems the JK Flip-Flop was developed.

The JK Flip-Flop is basically a Gated SR Flip-Flop with the addition of clock input circuitry that prevents the illegal or invalid output that can occur when both input S equals' logic level "1" and input R equals logic level "1". The symbol for a JK Flip-flop is similar to that of an SR Flip-Flop except for the addition of a clock input.

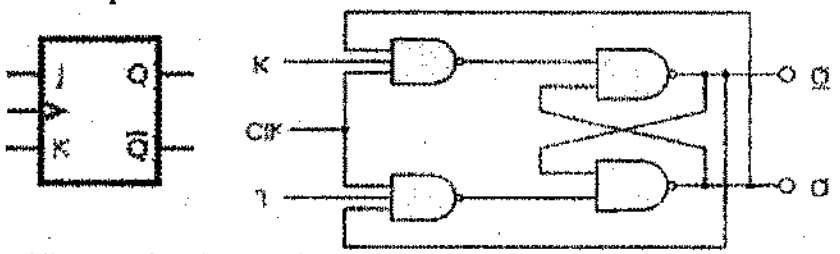


Figure 14.5: Symbolic and logic diagram of a JK Flip-Flop.

Table 14.2: Truth table of JK Flip-Flop.

Inputs			Output	Operation mode
Q_n	S	R	Q_{n+1}	
0	0	0	Q_n	No Change state
0	1	0	1	Set
1	0	0	1	No Change state after S=1 and R=0
1	0	1	0	Reset state
0	0	0	0	No Change state after S=0 and R=1
0	1	1	$\overline{Q}_n$	Compliment

Both the S and the R inputs of the SR flip-flop are replaced by two inputs called the J and K inputs, respectively. The two 2-input NAND gates of the clocked SR Flip-Flop have now been replaced by two 3-input AND gates with the third input of each gate connected to the outputs Q and Q. This cross coupling of the SR Flip-flop allows the previously invalid condition of S = "1" and R = "1" state to be usefully used to turn it into a "Toggle action" as the two inputs are now interlocked. If the circuit is "**Set**" the J input is inhibited by the "0" status of the Q through the lower AND gate. If the circuit is "**Reset**" the K input is inhibited by the "0" status of Q through the upper AND gate. When both inputs J and K are equal to logic "1", the JK flip-flop changes state and the truth table for this is given above.

Interestingly the JK Flip-flop is basically an SR Flip-flop with feedback and which enables only one of its two input terminals, either Set or Reset at any one time thereby eliminating the invalid condition seen previously in the SR Flip-flop circuit. Also when both the J and the K inputs are at logic level "1" at the same time, and the clock input is pulsed either "HIGH" or "LOW" the circuit will "Toggle" from a Set state to a Reset state, or visa-versa. In this condition the JK Flip-flop is called the **T-type Flip-flop** when both terminals are "HIGH".

Although this circuit is an improvement on the clocked SR flip-flop it still suffers from timing problems called "race around condition" if the output Q changes state before the timing pulse of the clock input has time to go "OFF". For example let the inputs are J=K=1 and Q=0. When the pulse is applied, the output becomes=1, this change take place after a time interval equal to the gate propagation delay. Now J=1, K=1 and Q=1, and the pulse is still ON will changes the output to Q=0. Hence we must conclude that for the duration t_p of the pulse (Clk = 1), the output will oscillates back and forth between 0 and 1. At the end of the pulse (Clk = 0), the value of Q is ambiguous.

To avoid this the timing pulse period (t_p) must be kept as short as possible (high frequency). As this is sometimes is not possible with modern TTL IC's the much improved **Master-Slave JK Flip-flop** was developed. This eliminates all the timing problems by using two SR flip-flops connected together in series, one for the "Master" circuit, which triggers on the leading edge of the clock pulse and the other, the "Slave" circuit, which triggers on the falling edge of the clock pulse.

14.2.5 Master-Slave JK Flip-flop

The **Master-Slave Flip-Flop** is basically two JK flip-flops connected together in a series configuration with the outputs from Q and from the "Slave" flip-flop being fed back to the inputs of the "Master" with the outputs of the "Master" flip-flop being connected to the two inputs of the "Slave" flip-flop as shown below.

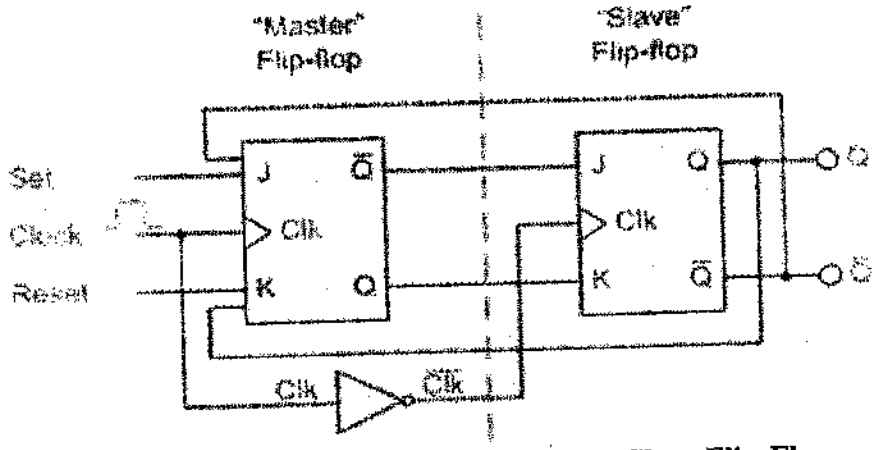


Figure 14.6: Logic diagram of a JK Master-Slave Flip-Flop.

The input signals J and K are connected to the "Master" flip-flop which "locks" the input while the clock (Clk) input is high at logic level "1". As the clock input of the "Slave" flip-flop is the inverse (complement) of the "Master" clock input, the outputs from the "Master" flip-flop are only "seen" by the "Slave" flip-flop when the clock input goes "LOW" to logic level "0". Therefore on the "High-to-Low" transition of the clock pulse the locked outputs of the "Master" flip-flop are fed through to the JK inputs of the "Slave" flip-flop making this type of flip-flop edge or pulse-triggered. Then, the circuit accepts input data when the clock signal is "HIGH", and passes the data to the output on the falling-edge of the clock signal. In other words, the **Master-Slave JK Flip-flop** is a "Synchronous" device as it only passes data with the timing of the clock signal. The operation of the device can be understood with the help of the truth table given below. When both J and K are high i.e. J=K=1, the output will toggle between 1 and 0 for each applied clock pulse. Thus this circuit eliminates the problem of the race around condition.

Table 14.3: Truth table of Master-slave JK Flip-Flop

Inputs			Output	Operation mode
Q_n	S	R	Q_{n+1}	
0	0	0	Q_n	No Change state
0	1	0	1	Set
1	0	0	1	No Change state after S=1 and R=0
1	0	1	0	Reset state
0	0	0	0	No Change state after S=0 and R=1
0	1	1	$\overline{Q}_n$	Toggle

14.2.6 D–type Flip-Flop

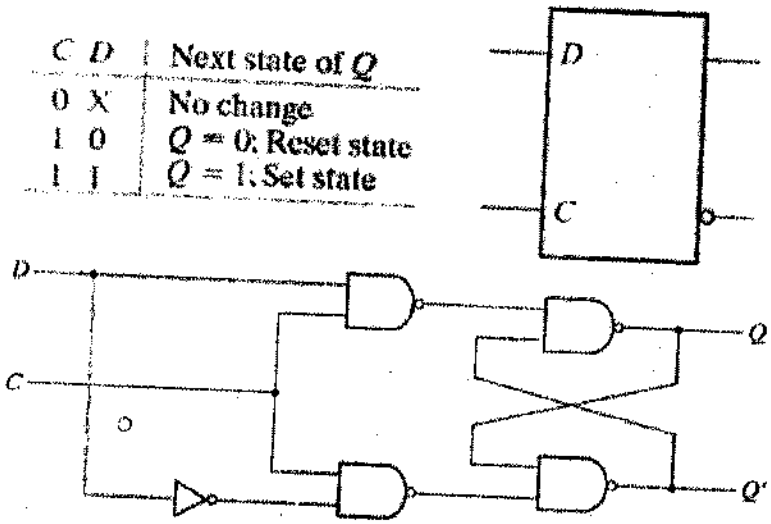


Figure 14.7: Symbol and logic diagram of a D type Flip-Flop.

If the SR flip-flop is modified by addition of an inverter as in figure, so that the inputs are compliment of each other, the circuit is called a D (delay) Flip-Flop. Thus the flip-flop using just one input as now the two latch inputs are complements of each other. $Q_{n+1}=1$ for $D_n=1$ (S==1) and $Q_{n+1}=0$ for D_n =S==0. The output Q_{n+1} after the pulse (bit time n+1) equals the input Dn before the pulse (bit time n). This single input is called the "DATA" input. If this data input is HIGH the flip-flop would be "SET" and when it is LOW the flip-flop would be "RESET". However, this would be rather pointless since the flip-flop's output would always change on every data input. To avoid this an additional input called the "CLOCK" or "ENABLE" input is used to isolate the data input from the flip-flop after the desired data has been stored. This circuit is also called delay type flip-flop because the output is delayed by the pulse.

14.2.7 T–type Flip-Flop

The T-type flip-flop changes state with each clock pulse, hence it acts as a toggle switch. If J=K=1, then $Q_{n+1}=_n$; so that the JK flip-flop is converted into a T-type Flip-flop. In Figure the T-type system is shown with a data input T and outputs.

Input	Output
T_n	Q_{n+1}
1	$\overline{Q}_n$
0	Q_n

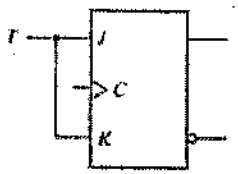


Figure 14.8: Logic symbol and truth table of a T-type flip-flop.

14.2.8 Excitation table and Characteristic Tables

In the designing of flip-flops and other digital circuits we usually know the transition from present state to next state and wish to find the flip-flop input conditions that will cause the required transition. For this reason, we need the tables that list the inputs and outputs as well as the required inputs for a given change of state. Such lists of tables are known as characteristics and excitation tables.

A characteristic table defined the logical property of the flip-flop and completely characterizes its operation in tabular form. In the flip-flops characteristic tables: Q_n refers to the present state prior to the application of a clock edge. Q_{n+1} are the next state after the occurrence of a clock pulse. The clock edge input is not included in the characteristic tables, but is implied to occur between time t and $t+1$.

Excitation table shows the minimum inputs that are necessary to generate a particular next state when the current state is known. They are similar to truth tables and state tables, but rearrange the data so that the current state and next state are next to each other on the left-hand side of the table, and the inputs needed to make that state change happen are shown on the right side of the table.

Table 1 presents the characteristic and excitation tables for the four FF's. In the excitation table there are two columns for Q_n and Q_{n+1}, and a column for each input to show how the required transition is achieved. There are four possible transitions from present state to next state. The required input conditions for each of the four transitions are derived from the information available in the characteristic table. The symbol "X" in the tables represents a don't-care condition, i.e., it does not matter whether the input is 1 or 0.

SR Flip-Flop

Characteristic Table				Excitation Table			
S	R	Q_{n+1} (next)	Comment	Q_n	Q_{n+1}(next)	S	R
0	0	0	Hold state	0	0	0	X
0	1	0	Reset	0	1	1	0
1	0	1	Set	1	0	0	1
1	1	?	Meta-stable	1	1	X	0

JK Flip-Flop

Characteristic Table				Excitation Table				
J	K	Q_{n+1} (next)	Comment	Q_n	Q_{n+1}(next)	J	K	Comment
0	0	Q_n	Hold state	0	0	0	X	Hold state
0	1	0	Reset	0	1	1	X	Set
1	0	1	Set	1	0	X	1	Reset
1	1	$\overline{Q}_n$	Toggle	1	1	X	0	Hold state

D-type Flip-Flop

Characteristic table		Excitation Table		
D	Q_{n+1} (next)	Q_n	Q_{n+1} (next)	D
0	0	0	0	0
		0	1	1
1	1	1	0	0
		1	1	1

In the D-type Flip-Flop, the next state is always equal to the D-input and independent of the present state. Therefore, D must be 0 if Q_{n+1} have to be 0 and 1 if Q_{n+1} have to be 1, regardless of the Q_n

T-type Flip-Flop

Characteristic table		Excitation Table		
T	Q_{n+1} (next)	Q_n	Q_{n+1} (next)	T
0	Q_n Hold	0	0	0
		0	1	1
1	$\bar{Q}_n$ Toggle	1	0	1
		1	1	0

In T-type flip-flop when T=1, the state of the flip-flop is complimented; when T=o, the state of the flip-flop remains unchanged. Therefore, same state of the flip-flop T has to be 0 and for complimented output T must be equal to 1.

14.2.9 Edge triggered Flip-Flops

Flip-flop is a digital system similar to a latch that possess two states and a feedback path that allows it to store a bit of information. The difference between a latch and a flip-flop is that a latch is asynchronous, and the outputs can change as soon as the inputs do (or at least after a small propagation delay). A flip-flop, on the other hand, is *edge-triggered* and only changes state when a control signal goes from high to low or low to high. The state of a flip-flop is switched by a momentary change in the input signal. This momentary change is called a trigger and the transition it causes is called trigger the flip-flop. For triggering the flip-flops generally clock pulses are used. A clock pulse may be either positive or negative. A positive clock source remains at 0 (low) during the interval between pulses and goes to 1 (high) during the occurrence of the pulse. A pulse goes through two signal transitions: from 0 to I and return from 1 to 0. Figure shows, the positive transition (known as positive edge) and the negative transition (known as negative edge). The same definition is allocable to negative or positive pulses as shown in the figure.

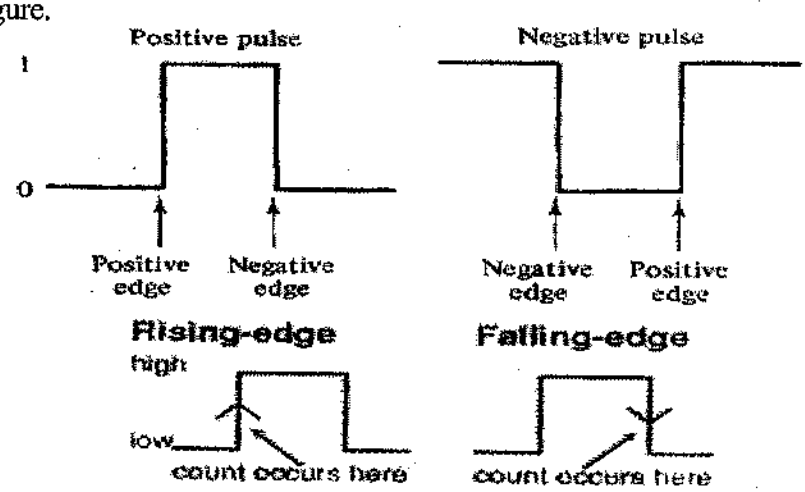


Figure 14.9: Definitions of clock pulse Transition.

The type of flip-flop that synchronizes the state changes during a clock pulse transition is called the edge- triggered flip-flop. In the edge-triggered flip-flop, the output transitions take place at a specific level of the clock. When the pulse input level exceeds the threshold level, the inputs are locked out and the flip-flop becomes unresponsive to further changes in the inputs until the clock pulse return to low and another pulse occurs. The graphic symbol for the edge-triggered *D* flip-flop is shown below.

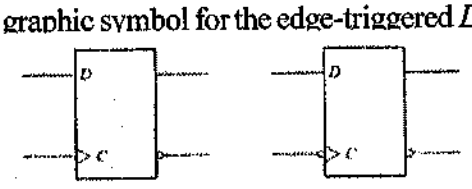


Figure:14.10: Symbolic diagram of positive and negative edge triggered D-type flip-flop.

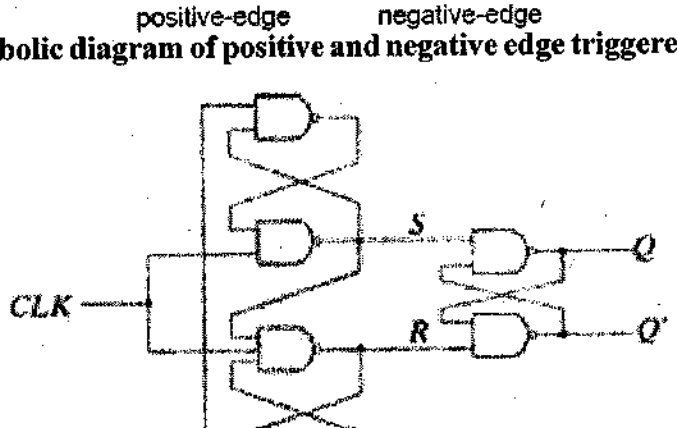


Figure 14.11: Logic diagram of an edge triggered D-type flip-flop.

14.3 REGISTERS

A register is group of binary storages units suitable for holding binary information. A group of clocked flip-flops constitutes a register. N-bit register has a group of n-flip-flops and capable of registering/storing information of n-bit. Figure shows a simple 4-bit register constructed using four D-type flip-flops and a common clock pulse input. The clock pulse enables all the flip-flops and the information presently available at the four D inputs (PA,PB,PC and PD) can be transferred into the four outputs (QA,QB,QC and QD) of the 4-bit register.

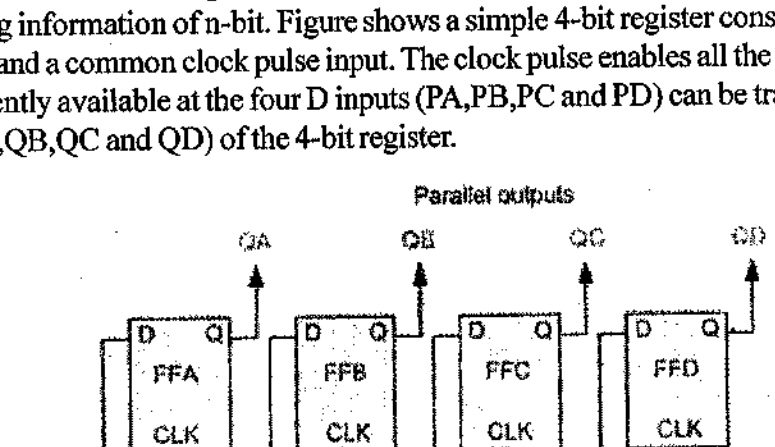


Figure 14.12: Logic diagram of a Register.

14.4 SHIFT REGISTERS

A shift register is a cascade of flip flops, triggered from the same clock pulse, which has the output of anyone but the last flip-flop connected to the "data" input of the next one in the chain, resulting in a circuit that shifts by one position the one-dimensional "bit array" stored in it, *shifting in* the data

present at its input and *shifting out* the last bit in the array, when enabled to do so by a transition of the clock input. Shift registers can have both parallel and serial inputs and outputs. These are often configured as serial-in and parallel-out or as parallel-in and serial-out. There are also types that have both serial and parallel input and types with serial and parallel output. There are also bi-directional shift registers which allow shifting in both directions: Left to right and right to left The serial input and last output of a shift register can also be connected together to create a circular shift register.

A shift register can be designed using number of single bit "D-Type Flip-flops" connected together in a chain arrangement so that the output from one data latch becomes the input of the next latch and so on, thereby moving the stored data serially from either the left or the right direction. A typical Serial-in to Parallel-out is shown below. The functioning of the circuit can be understand using the truth table, where with each pulse the value of the output shifts to the next stage. Initial value of 1010 output is shifted from left to right with clock-pulse.

Table 4: Serial data transfer using Shift register.

Timing pulse	QA	QB	QC	QD
Initial value	1	0	1	0
After T1	1	1	0	1
After T2	1	1	1	0
After T3	1	1	1	1
After T4	0	1	1	1

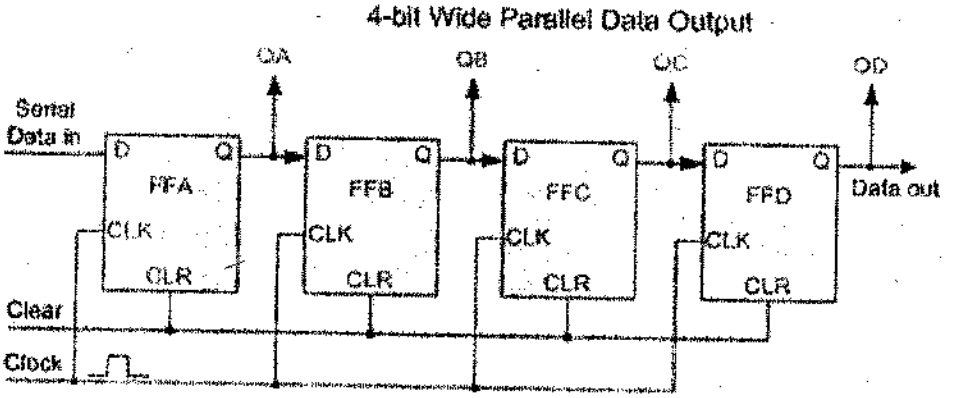


Figure 14.13: Four-bit Serial-in to Parallel-out Shift Register.

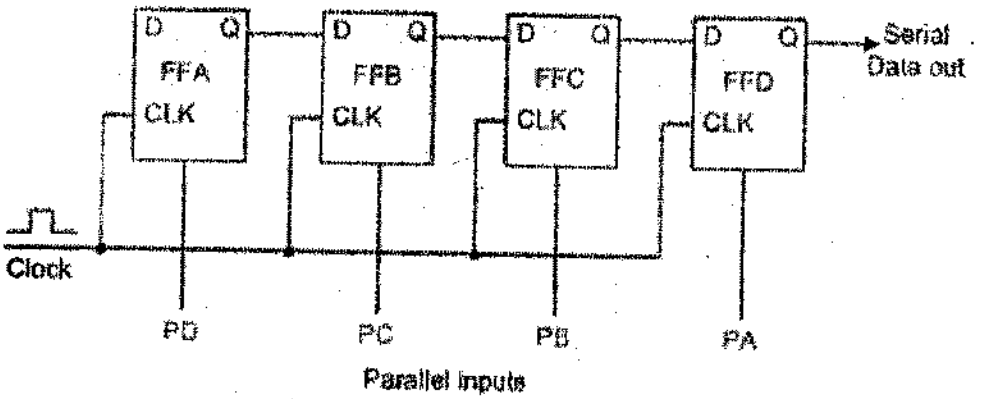


Figure 14.14: Four bit Parallel-in to serial-out Shift Register.

14.5 COUNTERS

Counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. There are two types of counters: asynchronous (ripple) and synchronous counters.

14.5.1 Ring counter

A ring counter can be designed using a shift register with the output of the last one connected to the input of the first, that is, in a ring. Typically a pattern consisting of a single 1 bit is circulated, so the

state repeats every N clock cycles if N flip-flops are used. It can be used as a cycle counter of N states.

The operation of a ring counter (shown below) can be understood with the help of following example. Let us assume that a starting state of $Q_3 = 1$ and $Q_2 = Q_1 = Q_0 = 0$. At the first pulse, the 1 shift from Q_3 to Q_2 and the counter is in the 0100 state. The next pulse produces the 0010 state and the third, 0001. At the fourth pulse, the 1 at Q_0 is transferred back to Q_3, resulting in the 1000 state, which is the initial state. Subsequent pulses will cause the sequence to repeat, hence the name ring counter.

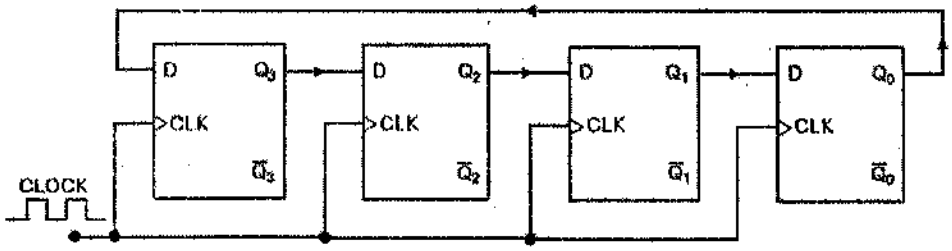


Figure 14.15: Logic diagram of ring counter designed using a shift register.

14.5.2 Asynchronous (ripple) Counters

An asynchronous or Binary ripple counter consists of a series of complementing flip-flops. In these counters the flip-flop output transition serves as a source for triggering other flip-flops. The clock inputs of all the flip-flops except the first are triggered not by incoming pulse but rather by output transition that occurs in other flip-flops. In a synchronous counter, the input pulses are allied to the clock inputs of all flip-flops. The change of state of a particular flip-flop is dependent on the present of other flip-flop. A binary counter consisting of n flip-flops has a count cycle of 2^n and counts from 0 to 2^n-1. A 4-bit binary ripple counter using T flip-flops is shown.

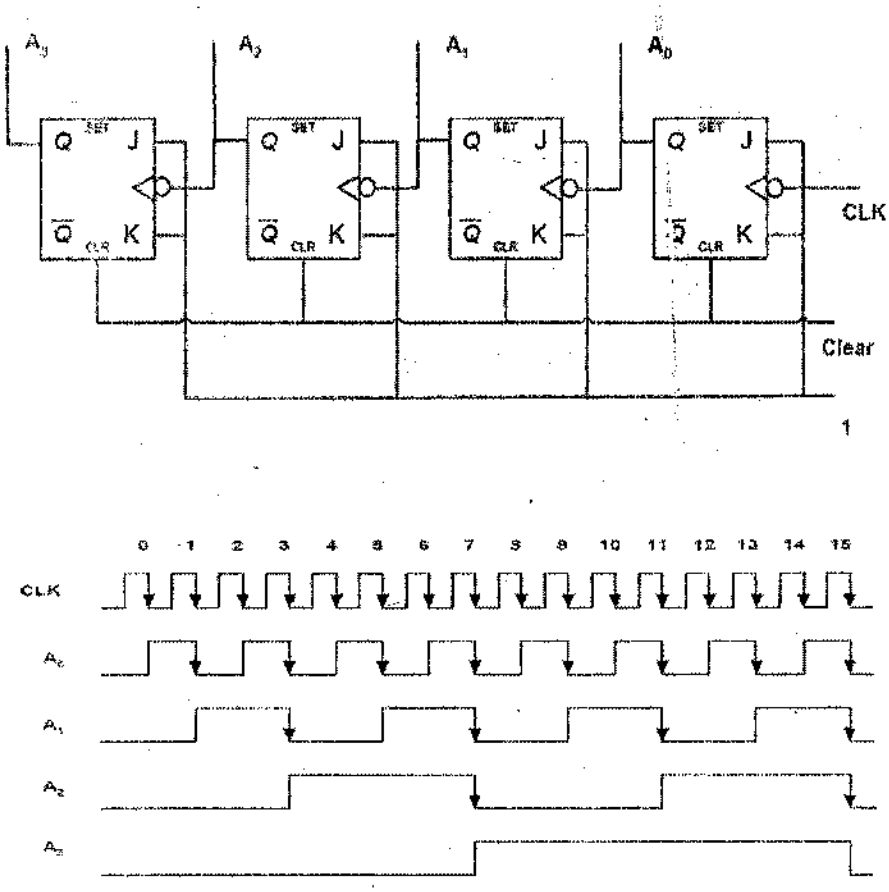


Figure 14.16: Block diagram and timing waveform chart for a 4-bit binary counter.

At the beginning let all the output are at 0. i.e. $A_4A_3A_2A_1 = 0000$. On the application of first clock pulse the output of first flip-flop will be complimented. Thus $A_4A_3A_2A_1 = 0001$. Second pulse make A_1 again at 0 but this transition from 1 to 0 will trigger the second flip-flop and make A_2 at 1. So that output will be $A_4A_3A_2A_1 = 0010$. Third pulse again trigger first flip flop. Therefore the output will be $A_4A_3A_2A_1 = 0011$. Applications of fourth pulse again compliment the first flip-flop and because of that both A_1 and A_2 will also changes their state which results change of state of A_3. So that $A_4A_3A_2A_1 = 0100$ and so on. The timing chart and truth tables for the 4-bit counter are given below.

Table 5: Functional table of a 4-bit binary ripple Counter.

S. No.	Input (pulses) Counts	Outputs (Binary)			
		A_3	A_2	A_1	A_0
1	0	0	0	0	0
2	1	0	0	0	1
3	2	0	0	1	0
4	3	0	0	1	1
5	4	0	1	0	0
6	5	0	1	0	1
7	6	0	1	1	0
8	7	0	1	1	1
9	8	1	0	0	0
10	9	1	0	0	1
11	10	1	0	1	0
12	11	1	0	1	1
13	12	1	1	0	0
14	13	1	1	0	1
15	14	1	1	1	0
16	15	1	1	1	1
17	16	0	0	0	0

14.5.3 Synchronous counter

A synchronous counter, in contrast to an asynchronous counter, is one whose output bits change state simultaneously, with no ripple. It can be designed using T-type flip-flops and the clock inputs of all the flip-flops is connected together, so that each and every flip-flop receives the exact same clock pulse at the exact same time. A synchronous binary counter counts from 0 to 2^N-1, where N is the number of bits/flip-flops in the counter. Each flip-flop is used to represent one bit. The flip-flop in the lowest-order position is complemented/toggled with every clock pulse and a flip-flop in any other position is complemented on the next clock pulse provided all the bits in the lower-order positions are equal to 1.

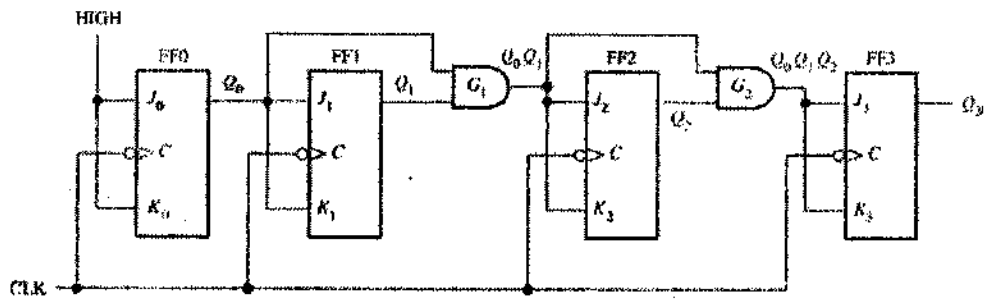


Figure 14.17: Circuit diagram of a 4-bit synchronous counter.

A 4-bit binary synchronous counter can be designed using T–type flip-flops and its operation can be

understood with help of the following example. Let all the four Flip-flops are $Q_4\ Q_3\ Q_2\ Q_1 = 0011$. On the next count, $Q_4\ Q_3\ Q_2\ Q_1 = 0100$. A_1, the lowest-order bit, is always complemented. Q_2 is complemented because all the lower-order positions (Q_1 only in this case) are 1's. Q_3 is also complemented because all the lower-order positions, Q_2 and Q_1 are 1's. But Q_4 is not complemented the lower-order positions, $Q_3\ Q_2\ Q_1 = 011$, do not give an all 1 condition.

Table 6: Functional table for a 4-bit synchronous counter.

S. No.	Input (pulses) Counts	Outputs (Binary)			
		Q_3	Q_2	Q_1	Q_0
1	0	0	0	0	0
2	1	0	0	0	1
3	2	0	0	1	0
4	3	0	0	1	1
5	4	0	1	0	0
6	5	0	1	0	1
7	6	0	1	1	0
8	7	0	1	1	1
9	8	1	0	0	0
10	9	1	0	0	1
11	10	1	0	1	0
12	11	1	0	1	1
13	12	1	1	0	0
14	13	1	1	0	1
15	14	1	1	1	0
16	15	1	1	1	1
17	16	0	0	0	0

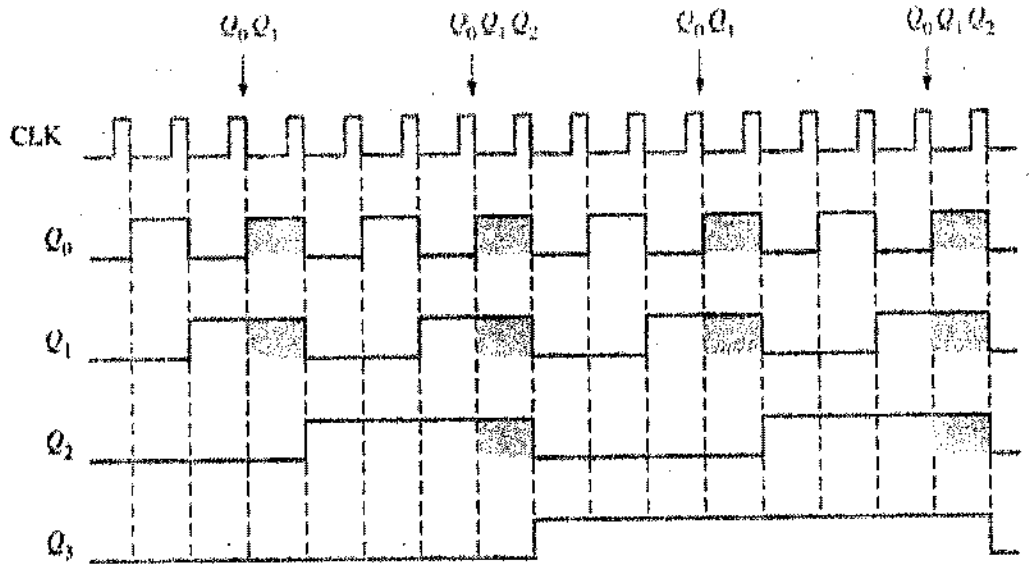


Figure 14.18: Wave-form charts for a 4-bit synchronous counter.

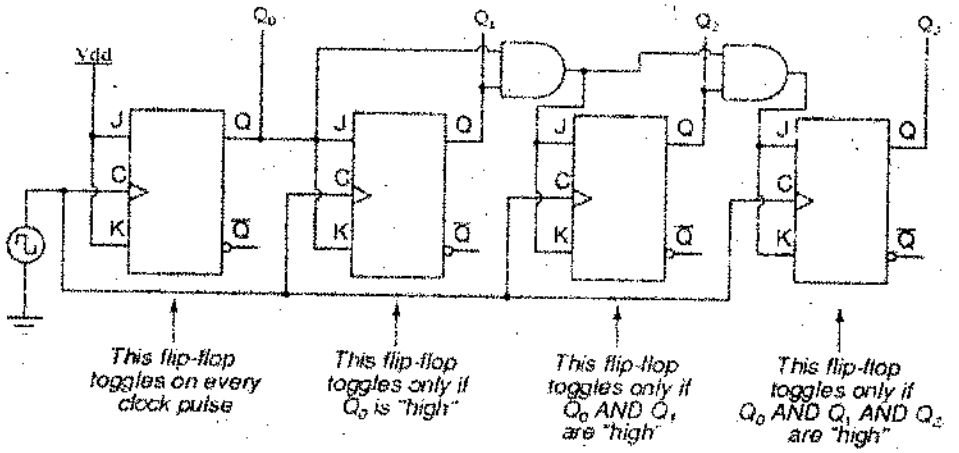


Figure 14.19: Circuit diagram of a 4-bit synchronous up counter.

In practice, counters can also classified to as Up counters, which increase (increment) in value and Down counters, which decrease (decrement) in value. A counter that can change state in either direction, under control an up–down selector input, is known as an up–down counter. When the selector is in the up state, the counter increments its value; when the selector is in the down state, the counter decrements the count. The circuit diagrams of up and down counters are shown below.

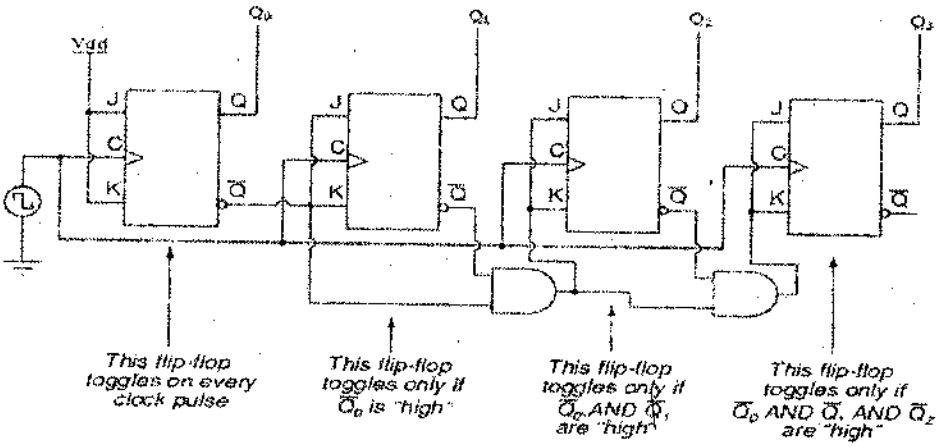


Figure 14.20: Circuit diagram of a 4-bit synchronous down counter.

14.6 REVIEW QUESTIONS

Q.1. What is a Flip-Flop? Draw the circuit of a Latch explain its operation.
Q.2. Draw the circuit of a SR Flip-Flop and explain its operation.
Q.3. Draw the circuit of a JK Flip-Flop and explain its operation.
Q.4. What do you mean by race around condition? Draw the circuit of a JK Master Slave Flip-Flop and explain its operation.
Q.5. Draw the circuit of a D-type Flip-Flop and explain its operation.
Q.6. Draw the circuit of a T-type Flip-Flop and explain its operation.
Q.7. Explain the 4-bit shift register.
Q.8. Explain the utility of ring counter.
Q.9. Draw the circuit of a ripples counter and explain its operation using suitable wave-form chart.
Q.10. Draw the circuit of a synchronous counter and explain its operation.
Q.11. Differentiate between asynchronous and synchronous counters